Voodoo3®

HIGH PERFORMANCE

GRAPHICS ENGINE

FOR

3D GAME ACCELERATION

Data Book: Revision 1.9

August 24, 1999

3dfx Interactive, Inc.
4435 Fortran Drive
San Jose CA 95134
Phone: (408) 935-4400
Fax: (408) 935-4424

Notice:
3dfx Interactive, Inc. has made best efforts to ensure that the information contained in this document is accurate and reliable. The information is subject to change without notice. No responsibility is assumed by 3dfx Interactive, Inc. for the use of this information, nor for infringements of patents or the rights of third parties. This document is the property of 3dfx Interactive, Inc. and implies no license under patents, copyrights, or trade secrets.

Trademarks:
All trademarks are the property of their respective owners.

Copyright Notice:

Proprietary Information:

Preliminary Data:
3dfx Interactive, Inc. has made best efforts to ensure that the information contained in this document is accurate.

Table of Contents

List of Tables

List of Figures

1 Introduction

1.1 Scope of Document

This is the Data Book for Voodoo3. This document includes a device overview, pin descriptions, DC and AC parameters, and additional information necessary to design with Voodoo3.

1.2 Document History

Table 1.1 Document History

Version	Date	Change from previous version
1.0	Sept. 29, 1998	Initial Version
1.1	Oct 19, 1998	GPIO0/GPIO1 descriptions corrected.
1.2	Oct 20, 1998	Serial Port connections on reference design corrected.
1.3	Nov 11, 1998	Corrected Serial port connections again.
1.4	Nov 17, 1998	Changed name to Voodoo3.
1.5	Dec 16, 1998	Changed RSET resistor value to 56.2 ohms
1.6	Feb 16, 1999	Corrected pllCtrl, AGP_PLL Strapping
1.7	Feb 22, 1999	Note added to GPIO[0] in pin descriptions, GPIO Notes
1.8	May 5, 99	Changed to new logo, companyname (correct print date)
1.9	Aug 24, 1999	Added Power Supply Limits, Thermal Characteristics

1.3 Devices Covered

This document covers the production version(s) of Voodoo3 - 250 and Voodoo3 - 333.

1.4 Audience

This document is tailored to a knowledgeable audience. It is assumed that the reader is familiar with assembly language programming of Pentium® CPU and has a good foundation in computer-generated graphics, especially 3D.
Hardware designers intending to use Voodoo3 should have experience in the design of mixed analog-digital devices with very high bandwidth buses. Some signals have fast edge rates and will behave as transmission lines, requiring controlled impedance traces and short, direct connections. Experience with SGRAM/SDRAM arrays and the PCI/AGP bus will be valuable. Designers are encouraged to study the layout guidelines available from 3dfx Interactive, Inc.

1.5 Conventions

1.5.1 Acronyms

The first appearance of each TLA (Three Letter Acronym) is followed immediately by the definition in parentheses.

1.5.2 Number Base

Hexadecimal (base 16) numbers use upper case letters ABCDEF. Hexadecimal numbers have a

prepended ‘0x’ or an appended ‘h’. The following are examples of hexadecimal numbers: 0x00, 0x3DF, 3DFh, 0x1234, 0x2A. Eight-digit hexadecimal numbers typically contain a space in the middle. For example 0x0123 4567 is an eight-digit hexadecimal number.
Decimal (base 10) numbers have no special indicator. The following are examples of decimal numbers: 1234, 2380, 42.
Binary (base 2) have an appended ‘b’. The following are examples of binary numbers: 00b, 01b, 101010b.
Octal (base 8) numbers are not used in this document.
The value zero is often written as 0, without any quotes and without indication as to size or base.

1.5.3 Object Grouping

Objects that are grouped together are listed in descending order. A range is indicated with surrounding square brackets and a colon between the highest and the lowest in the range. A[7:0] means A7, A6, A5, A4, A3, A2, A1, A0. This convention is used for bits in a register (for example, CR2[7:0]) and for signal pins (for example, PCI_AD[31:0]).

1.5.4 Abbreviations

The following abbreviations are used in this document.

Table 1.2 Abbreviations

Abbreviation	Meaning	Note
Kbyte	1024 bytes	
Mbyte	1,048,576 bytes	1024 Kbytes
Gbyte	1,073,741,824 bytes	1024 Mbytes
Hz	Hertz	frequency
kHz	1000 Hertz	
MHz	1,000,000 Hertz	
ms	10^{-3} second	period
us	10^{-6} second	
ns	10^{-9} second	
mA	10^{-3} Ampere	current
uA	10^{-6} Ampere	
uF	10^{-6} Farad	capacitance
pF	10^{-12} Farad	
tbd, na	To Be Determined, Not Available	used interchangeably
Mpixel	1,000,000 pixels	

2 Product Overview

2.1 Introduction

Voodoo3 incorporates leading-edge 3D graphics and extremely fast 128-bit Windows® GUI/Video Acceleration into a single chip.

2.1.1 Voodoo Graphics Compatibility

Since Voodoo3 is upward compatible with Voodoo® 3D, hundreds of 3D titles that have been optimized for acceleration on Voodoo Graphics, Voodoo Rush, Voodoo^2, and Voodoo Banshee will run on Voodoo3 without modification. Of course, to take advantage of the Voodoo3 enhanced features, it will be necessary make changes.

2.1.2 3D Performance and Quality

3dfx Interactive, Inc. is the industry leader in delivering 3D technology for the PC consumer market. Voodoo3 - 333 will continue this heritage, delivering 333 Mtexels/sec and over 6 million triangles per second single-cycle multi-texturing 3D performance[1]. The design philosophy behind all products of 3dfx Interactive, Inc. is to provide advanced 3D features with the universal requirement of all serious game developers: **no degradation in performance and quality**. As an example, Voodoo3 provides per-pixel level-of-detail MIP mapping and per-pixel atmospheric effects such as fog and haze. Other solutions that provide these features at all do so on a per-polygon basis, yielding an inferior image.

2.1.3 Optimized for Pentium® II and AGP-2X Platform

Voodoo3 is the only solution to fully exploit the processing power the Pentium® II, including direct hardware handling of out-of-order writes. From the very beginning, Voodoo3 was designed to maximize the performance of the Pentium Pro and Pentium II I/O architecture. The AGP interface is tuned for optimal 3D performance, and supports sideband addressing for very fast texture downloading and full 2X 133 MHz AGP bus operation.

2.1.4 Windows® GUI/Video Acceleration

Voodoo3 - 333 is a 166 MHz (125 for the -250 product) single-cycle GUI accelerator with 128-bit frame buffer interface. Even the VGA core is 128 bits. The design philosophy has been to implement the Microsoft GDI (Graphics Device Interface) in hardware for outstanding windows acceleration. Voodoo3 supports the new features of Windows98 (for example, multi-monitor support) and is PC99 compliant.

2.1.5 DVD Acceleration

The video architecture of Voodoo3 is optimized for software DVD acceleration. This optimization includes large FIFOs, YUV 4:2:0 planar to packed pixel conversion with AGP bus-mastering, automatic double-buffering, and alpha blending for sub-picture support.

2.2 Feature List

2.2.1 General Features

- Two texels per clock
- Fully integrated 128-bit VGA/2D/3D/Video Accelerator
- 2X AGP with sideband addressing
- Fully software-compatible with 3Dfx Voodoo Banshee
- Floating point depth buffer (W buffer)
- Ultimate 3D experience with 333 Mtexels/sec and 6 million triangles/sec for - 333 product,
- 250 Mtexels and 4 million triangles/sec for - 250 product
- Hardware support for Out-of-order writes

1. The -250 product will deliver 250 Mtexel/sec and over 4 million triangles per second.

- Hardware DVD acceleration
- Digital video output for NTSC and PAL TV-out support
- DFP or VESA FPDI LCD support through external ASIC
- Full VMI (includes the host port) for Hardware DVD decoding or digital video capture
- HDTV resolution of 2132 x 1600 at 60 Hz with 350 MHz (-333 product) RAMDAC
- Supports 4-, 8-, 16-Mbyte SGRAM or 16-Mbyte SDRAM frame buffer
- PC99 rev 1.0 compliant
- VESA DDC2B support

2.2.2 2D Acceleration

- 333 MHz (250 for -250 product) single-cycle 128-bit Windows GUI acceleration
- Fully-featured 128-bit BitBlt Engine: Windows GDI in hardware
- Acceleration for Bresenham line draw, 2-edge polygon fill, scissor/rectangle clippers, 256 ROPs
- Source and destination chroma-keying for DirectDraw
- SGRAM color expansion support and single-cycle block writes
- Accelerated 8-, 16-, 24 (packed)-, 32-bpp modes

2.2.3 3D Acceleration

- Dual texture units: Two texels per-pixel per-clock
- Full hardware setup of triangle parameters
- Support for multi-triangle strips and fans
- 16-bit integer and floating-point Z-buffering with biasing
- Transparency and chroma-key with dedicated color mask
- Alpha blending of source and destination pixels
- Sub-pixel and sub-texel correction to 0.4 x 0.4 resolution
- 24-bit color dithering to native 16-bit RGB
- Per-pixel atmospheric fog with programmable fog zones
- Full-scene polygon-based edge anti-aliasing
- Dynamic environment mapping
- Perspective correct (true divide-per-pixel) 3D texture mapping and Gouraud shading
- Single-cycle bump mapping
- Single-cycle Trilinear Mip-mapping
- Anisotropic filtering
- True per-pixel LOD (level-of-detail) MIP mapping with biasing and clamping
- RGB modulation combines textures and shaded pixels
- Texture compositing for multi-texture special effects
- Support of 14 texture map formats
- 8-bit paletted textures with full bilinear filtering
- Texture compression through narrow-channel YAB format

2.2.4 Video Acceleration

- Multiple video window support
- Bilinear horizontal and vertical filtering
- YUV 4:2:2 and YUV 4:2:0 planar support
- De-interlacing using ‘bob’ and ‘weave’
- Automatic page flipping using VBI (Vertical Blanking Interval) for smooth motion video
- Triple 512 x 8 color lookup tables with separate gamma correction for video and graphics
- Separate gamma correction for video and graphics

2.2.5 Host Interface

- AGP 2X interface includes optimized support for sideband addressing
- PCI v2.1 bus interface supports 33 MHz and 66 MHz
- FIFO optimized for high speed bursting of geometry and texture data
- Optimized for Pentium II I/O architecture; out-of-order writes handled in hardware

- Bi-endian byte-ordering support

2.2.6 Memory System

- Advanced architecture with 3.0 Gbyte/sec (2.7 Gbyte/sec for -250 product) memory bandwidth
- 4 - 16 Mbytes of 166 MHz (125 for -250 product) and faster SGRAM/SDRAM

2.2.7 Process and Package Technology

- Custom IC fabricated in 0.25 micron, 5 metal layer CMOS
- 352-lead (plus 100 thermal ball) 35mm PBGA package
- 2.5 volt power with PCI and 5-volt tolerant I/O
- Built-in Iddq, CRC, and Parametric NAND tree for testability

2.2.8 Software

- Full BIOS and driver compatibility with Voodoo Banshee for a mature, robust solution
- Windows95, Windows98, WindowNT4.0 device drivers
- Extensive 3D API support including Glide 2.X and 3.X, OpenGL ICD, Microsoft D3D
- Support for TV encoders: Chrontel 7004, Brooktree 868/9
- Software DVD support: Quadrant

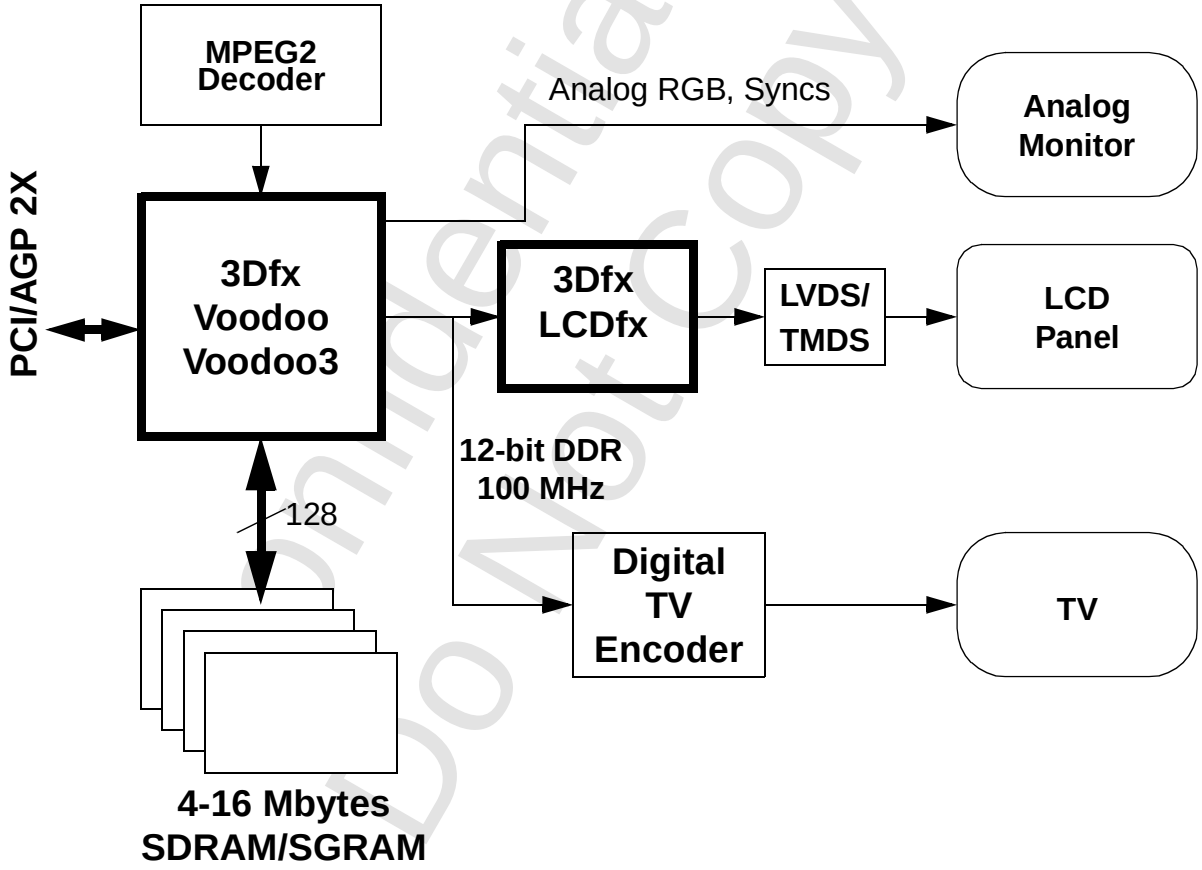


Figure 2.1 System Block Diagram

3 Pins

3.1 Introduction

The Voodoo3 pins are described in this chapter. Included are pin diagrams, pin tables, and detailed pin descriptions. Where appropriate, the detailed pin descriptions include board design notes.

3.2 Pin Diagrams

Voodoo3 is available in a 452-lead PBGA (352 leads and 100 thermal balls). Figure 3.1 is a high-level diagram showing the buses for reference only. Table 3.1 is the detailed pin diagram.

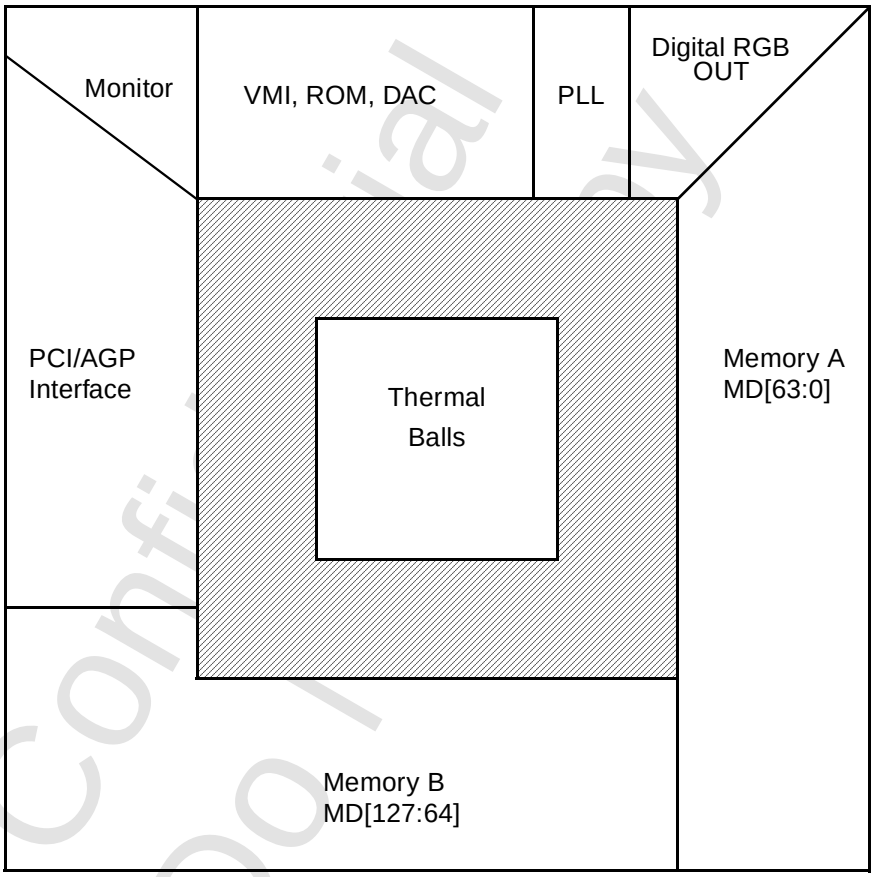
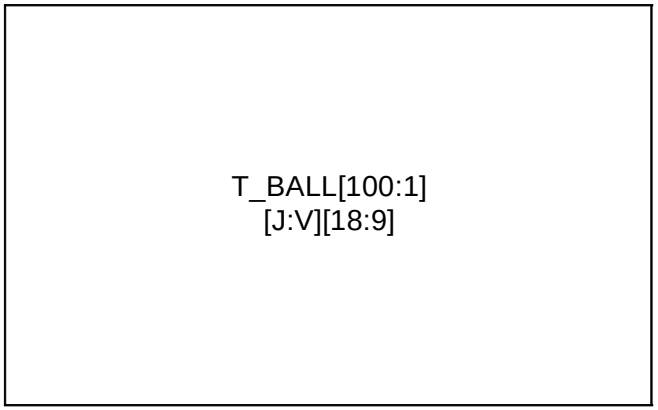


Figure 3.1 Bus Diagram

Table 3.1 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSYNC	IDDQ	HSYNC	GPIO0	ROMOE	VINT	VRDY	VRW	VCS	VHD0	DAVSS	GREEN	VCC_C	VHA0	PD6	PD2	PD1	PAVSS0	XIN	TBLNK	THSYNC	TVD8	TVD5	TVD1	MD31	MD3
B	INTA	RST	SDA0	GPIO1	SDC1	ROMCS	VRST	VDS	VHA3	DAVSSR	DRSET	BLUE	VHA2	VVSYNC	PD7	PD3	PCLK	PAVDD0	PAVSS1	TCLKO	TVD11	TVD7	TVD4	TVD2	TVD0	MD1
C	PGNT	ST0	SDC0	GPIO2	ROMWE	VHD6	VHD4	VHD3	VHD1	VBG	DAVDDI	VHA1	VPCLK	VBLNK	PD4	PD0	APVSS	XOUT	PAVDD1	TRST	TVD10	TVD6	TVD3	MD2	MD30	MD0
D	RBF	ST2	ST1	GND	SDA1	VHD7	VHD5	VCC	VHD2	GND	DAVDD	RED	CLKO	VHSYNC	VCC_C	PD5	GND	APVDD	VCC	TICLK	TVSYNC	TVD9	GND	MD29	MD4	MD5
E	SBA2	SBA1	SBA0	SBA3																		(E)	MD7	MD27	MD6	MD28
F	SBA5	SBA4	SBSTB	SBA6																		(F)	MD16	MD20	MD18	MD17
G	PAD30	PAD31	SBA7	PAD29																		(G)	MD19	MD24	MD21	MD26
H	PAD26	PAD27	PAD28	VCC																		(H)	VCC	MD23	MD25	MD22
J	ADSTB1	PAD24	PAD25	PAD23																		(J)	MDM0	MWEA	MD15	MDM2
K	PAD21	IDSEL	CBE3	GND																		(K)	GND	MD14	MRASA	MCASA
L	PAD20	PAD19	PAD22	PAD17																		(L)	MD13	MD12	MA_A9	MA_A10
M	AVREF	CBE2	PAD18	PAD16																		(M)	MD11	MD10	MA_A1	MA_A0
N	FRAME	IRDY	VCC_C	DEVSEL																		(N)	MA_A2	MD8	MD9	MA_A3
P	VCC_C	STOP	TDRY	PAR																		(P)	MA_A4	MDM3	MA_A5	VCC_C
R	PAD14	PAD15	CBE1	PAD13																		(R)	MA_A6	MDM6	MDM1	MA_A7
T	PAD10	PAD11	PAD12	PAD9																		(T)	MA_A8	MDM4	VCC_C	MDSFA
U	CBE0	PAD8	VCC_C	GND																		(U)	GND	MD54	MD53	MD55
V	PAD6	PAD7	ADSTB0	PAD5																		(V)	MCLKA	MD52	MD51	MCLKAI
W	PAD2	PAD3	PAD4	VCC																		(W)	VCC	MD50	MDM5	MDM7
Y	MD127	PAD0	PAD1	MD97																		(Y)	MD41	MD49	MD48	MD40
AA	MD126	MD125	MD96	MD98																		(AA)	MD43	MD45	MD39	MD42
AB	MD122	MD124	MD123	MD121	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	(AB)	MD44	MD47	MD38	MD37
AC	MD111	MD110	MD120	GND	MCLKBI	MD116	MD115	VCC	MD118	GND	MA_B0	MA_B10	MCASB	MD76	MD87	MD85	GND	MD90	VCC	MD68	MD65	MD62	GMD	MD36	MD35	MD46
AD	MD108	MD109	MD100	MD104	MD113	MD114	MA_B7	MA_B5	MA_B3	MA_B1	MDM12	VCC_C	MWEB	MRASB	MDM10	MD86	MD84	MD83	MD80	MD92	MD93	MD64	MD32	MD60	MD57	MD56
AE	MD101	MD106	MD103	MDM15	MD102	MD112	MA_B8	MA_B6	MA_B4	MA_B2	MDM9	MA_B9	(nc)	MD75	MDM8	MD78	MD88	MD82	MD71	MD69	MD66	MD63	MD95	MD61	MD59	MD34
AF	MD99	MD107	MD105	MDM13	MCLKB	MDSFB	MD117	MD119	MDM14	MDM11	MD73	MD72	MD74	VCC_C	MD77	MD79	MD89	MD81	MD70	MD91	MD67	MD94	MD33	MCS1	MCS0	MD58



3.3 Pin Tables

The following tables contain pin names, pin number, pin type, and a brief description. The pins are organized into the groups shown in Table 3.2.
Within each group, the pins are listed in alphabetical order, higher number first. Because of space limitations in the pin diagram (Table 3.1), it was necessary to abbreviate some pin names. The abbreviated names are in the second column of each table.

Table 3.2 Pin Table Summary

Group	Table	Link
PCI Interface	Table 3.3	Section 3.4.1
AGP Interface	Table 3.4	Section 3.4.2
Frame Buffer Memory	Table 3.5	Section 3.4.3
Monitor Interface	Table 3.6	Section 3.4.4
VMI Interface	Table 3.7	Section 3.4.5
Digital RGB Out	Table 3.8	Section 3.4.6
Miscellaneous	Table 3.9	Section 3.4.7
Power and Ground	Table 3.10	Section 3.4.8

Table 3.3 PCI Interface Signals

Name	Abbr. Name	Position	Type	Description
PCI_AD31	PAD31	G2	I/O	PCI Address and Data Bus
PCI_AD30	PAD30	G1	I/O	PCI Address and Data Bus
PCI_AD29	PAD29	G4	I/O	PCI Address and Data Bus
PCI_AD28	PAD28	H3	I/O	PCI Address and Data Bus
PCI_AD27	PAD27	H2	I/O	PCI Address and Data Bus
PCI_AD26	PAD26	H1	I/O	PCI Address and Data Bus
PCI_AD25	PAD25	J3	I/O	PCI Address and Data Bus
PCI_AD24	PAD24	J2	I/O	PCI Address and Data Bus
PCI_AD23	PAD23	J4	I/O	PCI Address and Data Bus
PCI_AD22	PAD22	L3	I/O	PCI Address and Data Bus
PCI_AD21	PAD21	K1	I/O	PCI Address and Data Bus
PCI_AD20	PAD20	L1	I/O	PCI Address and Data Bus

Table 3.3 PCI Interface Signals (Continued)

Name	Abbr. Name	Position	Type	Description
PCI_AD19	PAD19	L2	I/O	PCI Address and Data Bus
PCI_AD18	PAD18	M3	I/O	PCI Address and Data Bus
PCI_AD17	PAD17	L4	I/O	PCI Address and Data Bus
PCI_AD16	PAD16	M4	I/O	PCI Address and Data Bus
PCI_AD15	PAD15	R2	I/O	PCI Address and Data Bus
PCI_AD14	PAD14	R1	I/O	PCI Address and Data Bus
PCI_AD13	PAD13	R4	I/O	PCI Address and Data Bus
PCI_AD12	PAD12	T3	I/O	PCI Address and Data Bus
PCI_AD11	PAD11	T2	I/O	PCI Address and Data Bus
PCI_AD10	PAD10	T1	I/O	PCI Address and Data Bus
PCI_AD9	PAD9	T4	I/O	PCI Address and Data Bus
PCI_AD8	PAD8	U2	I/O	PCI Address and Data Bus
PCI_AD7	PAD7	V2	I/O	PCI Address and Data Bus
PCI_AD6	PAD6	V1	I/O	PCI Address and Data Bus
PCI_AD5	PAD5	V4	I/O	PCI Address and Data Bus
PCI_AD4	PAD4	W3	I/O	PCI Address and Data Bus
PCI_AD3	PAD3	W2	I/O	PCI Address and Data Bus
PCI_AD2	PAD2	W1	I/O	PCI Address and Data Bus
PCI_AD1	PAD1	Y3	I/O	PCI Address and Data Bus
PCI_AD0	PAD0	Y2	I/O	PCI Address and Data Bus
PCI_CBE3	CBE3	K3	Input	PCI Command and Byte Enables
PCI_CBE2	CBE2	M2	Input	PCI Command and Byte Enables
PCI_CBE1	CBE1	R3	Input	PCI Command and Byte Enables
PCI_CBE0	CBE0	U1	Input	PCI Command and Byte Enables
PCI_CLK	PCLK	B17	Input	PCI Clock
PCI_DEVSEL	DEVSEL	N4	I/O	PCI Device Select
PCI_FRAME	FRAME	N1	Input	PCI Transfer Frame
PCI_GNT_N	PGNT	C1	Input	PCI Bus Grant

Table 3.3 PCI Interface Signals (Continued)

Name	Abbr. Name	Position	Type	Description
PCI_IDSEL	IDSEL	K2	Input	PCI Initialization Device Select
PCI_INTA_N	INTA	B1	Output	PCI Interrupt Request
PCI_IRDY_N	IRDY	N2	Input	PCI Initiator Ready
PCI_PAR	PAR	P4	I/O	PCI Bus Parity
PCI_RESET_N	RST	B2	Input	PCI System Reset
PCI_STOP_N	STOP	P2	Output	PCI Transfer Stop
PCI_TRDY_N	TRDY	P3	I/O	PCI Target Ready

Table 3.4 AGP Interface Signals

Name	Abbr. Name	Position	Type	Description
AGP_AD_STB1	ADSTB1	J1	Input	AD Bus Strobe 1
AGP_AD_STB0	ADSTB0	V3	Input	AD Bus Strobe 0
AGP_RBF_N	RBF	D1	Output	AGP Read Buffer Full
AGP_SB_STB	SBSTB	F3	Output	AGP Sideband Strobe
AGP_SBA7	SBA7	G3	Output	AGP Sideband Address Bus
AGP_SBA6	SBA6	F4	Output	AGP Sideband Address Bus
AGP_SBA5	SBA5	F1	Output	AGP Sideband Address Bus
APG_SBA4	SBA4	F2	Output	AGP Sideband Address Bus
AGP_SBA3	SBA3	E4	Output	AGP Sideband Address Bus
AGP_SBA2	SBA2	E1	Output	AGP Sideband Address Bus
AGP_SBA1	SBA1	E2	Output	AGP Sideband Address Bus
AGP_SBA0	SBA0	E3	Output	AGP Sideband Address Bus
AGP_ST2	ST2	D2	Input	AGP Status Bus
AGP_ST1	ST1	D3	Input	AGP Status Bus
AGP_ST0	ST0	C2	Input	AGP Status Bus
AGP_VREF	AVREF	M1	Wire	AGP Voltage Reference

Table 3.5 Frame Buffer Memory Signals

Name	Abbr. Name	Position	Type	Description
MA_A10	MA_A10	L26	Output	Frame Buffer Port A Address
MA_A9	MA_A9	L25	Output	Frame Buffer Port A Address
MA_A8	MA_A8	T23	Output	Frame Buffer Port A Address
MA_A7	MA_A7	R26	Output	Frame Buffer Port A Address
MA_A6	MA_A6	R23	Output	Frame Buffer Port A Address
MA_A5	MA_A5	P25	Output	Frame Buffer Port A Address
MA_A4	MA_A4	P23	Output	Frame Buffer Port A Address
MA_A3	MA_A3	N26	Output	Frame Buffer Port A Address
MA_A2	MA_A2	N23	Output	Frame Buffer Port A Address
MA_A1	MA_A1	M25	Output	Frame Buffer Port A Address
MA_A0	MA_A0	M26	Output	Frame Buffer Port A Address
MA_B10	MA_B10	AC12	Output	Frame Buffer Port B Address
MA_B9	MA_B9	AE12	Output	Frame Buffer Port B Address
MA_B8	MA_B8	AE7	Output	Frame Buffer Port B Address
MA_B7	MA_B7	AD7	Output	Frame Buffer Port B Address
MA_B6	MA_B6	AE8	Output	Frame Buffer Port B Address
MA_B5	MA_B5	AD8	Output	Frame Buffer Port B Address
MA_B4	MA_B4	AE9	Output	Frame Buffer Port B Address
MA_B3	MA_B3	AD9	Output	Frame Buffer Port B Address
MA_B2	MA_B2	AE10	Output	Frame Buffer Port B Address
MA_B1	MA_B1	AD10	Output	Frame Buffer Port B Address
MA_B0	MA_B0	AC11	Output	Frame Buffer Port B Address
MCAS_A	MCACA	K26	Output	Frame Buffer Port A CAS
MCAS_B	MCASB	AC13	Output	Frame Buffer Port B CAS
MCLKA	MCLKA	V23	Output	Frame Buffer Port A Clock Out
MCLKA_IN	MCLKAI	V26	Input	Frame Buffer Port A Clock Feedback
MCLKB	MCLKB	AF5	Output	Frame Buffer Port B Clock Out

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MCLKB_IN	MCLKBI	AC5	Input	Frame Buffer Port B Clock Feedback
MCS_1	MCS1	AF24	Output	Frame Buffer Bank 1 Chip Select
MSC_0	MCS0	AF25	Output	Frame Buffer Bank 0 Chip Select
MD127	MD127	Y1	I/O	Frame Buffer Data Bus
MD126	MD126	AA1	I/O	Frame Buffer Data Bus
MD125	MD125	AA2	I/O	Frame Buffer Data Bus
MD124	MD124	AB2	I/O	Frame Buffer Data Bus
MD123	MD123	AB3	I/O	Frame Buffer Data Bus
MD122	MD122	AB1	I/O	Frame Buffer Data Bus
MD121	MD121	AB4	I/O	Frame Buffer Data Bus
MD120	MD120	AC3	I/O	Frame Buffer Data Bus
MD119	MD119	AF8	I/O	Frame Buffer Data Bus
MD118	MD118	AC9	I/O	Frame Buffer Data Bus
MD117	MD117	AF7	I/O	Frame Buffer Data Bus
MD116	MD116	AC6	I/O	Frame Buffer Data Bus
MD115	MD115	AC7	I/O	Frame Buffer Data Bus
MD114	MD114	AD6	I/O	Frame Buffer Data Bus
MD113	MD113	AD5	I/O	Frame Buffer Data Bus
MD112	MD112	AE6	I/O	Frame Buffer Data Bus
MD111	MD111	AC1	I/O	Frame Buffer Data Bus
MD110	MD110	AC2	I/O	Frame Buffer Data Bus
MD109	MD109	AD2	I/O	Frame Buffer Data Bus
MD108	MD108	AD1	I/O	Frame Buffer Data Bus
MD107	MD107	AF2	I/O	Frame Buffer Data Bus
MD106	MD106	AE2	I/O	Frame Buffer Data Bus
MD105	MD105	AF3	I/O	Frame Buffer Data Bus
MD104	MD104	AD4	I/O	Frame Buffer Data Bus
MD103	MD103	AE3	I/O	Frame Buffer Data Bus

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MD102	MD102	AE5	I/O	Frame Buffer Data Bus
MD101	MD101	AE1	I/O	Frame Buffer Data Bus
MD100	MD100	AD3	I/O	Frame Buffer Data Bus
MD99	MD99	AF1	I/O	Frame Buffer Data Bus
MD98	MD98	AA4	I/O	Frame Buffer Data Bus
MD97	MD97	Y4	I/O	Frame Buffer Data Bus
MD96	MD96	AA3	I/O	Frame Buffer Data Bus
MD95	MD95	AE23	I/O	Frame Buffer Data Bus
MD94	MD94	AF22	I/O	Frame Buffer Data Bus
MD93	MD93	AD21	I/O	Frame Buffer Data Bus
MD92	MD92	AD20	I/O	Frame Buffer Data Bus
MD91	MD91	AF20	I/O	Frame Buffer Data Bus
MD90	MD90	AC18	I/O	Frame Buffer Data Bus
MD89	MD89	AF17	I/O	Frame Buffer Data Bus
MD88	MD88	AE17	I/O	Frame Buffer Data Bus
MD87	MD87	AC15	I/O	Frame Buffer Data Bus
MD86	MD86	AD16	I/O	Frame Buffer Data Bus
MD85	MD85	AC16	I/O	Frame Buffer Data Bus
MD84	MD84	AD17	I/O	Frame Buffer Data Bus
MD83	MD83	AD18	I/O	Frame Buffer Data Bus
MD82	MD82	AE18	I/O	Frame Buffer Data Bus
MD81	MD81	AF18	I/O	Frame Buffer Data Bus
MD80	MD80	AD19	I/O	Frame Buffer Data Bus
MD79	MD79	AF16	I/O	Frame Buffer Data Bus
MD78	MD78	AE16	I/O	Frame Buffer Data Bus
MD77	MD77	AF15	I/O	Frame Buffer Data Bus
MD76	MD76	AC14	I/O	Frame Buffer Data Bus
MD75	MD75	AE14	I/O	Frame Buffer Data Bus

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MD74	MD74	AF13	I/O	Frame Buffer Data Bus
MD73	MD73	AF11	I/O	Frame Buffer Data Bus
MD72	MD72	AF12	I/O	Frame Buffer Data Bus
MD71	MD71	AE19	I/O	Frame Buffer Data Bus
MD70	MD70	AF19	I/O	Frame Buffer Data Bus
MD69	MD69	AE20	I/O	Frame Buffer Data Bus
MD68	MD68	AC20	I/O	Frame Buffer Data Bus
MD67	MD67	AF21	I/O	Frame Buffer Data Bus
MD66	MD66	AE21	I/O	Frame Buffer Data Bus
MD65	MD65	AC21	I/O	Frame Buffer Data Bus
MD64	MD64	AD22	I/O	Frame Buffer Data Bus
MD63	MD63	AE22	I/O	Frame Buffer Data Bus
MD62	MD62	AC22	I/O	Frame Buffer Data Bus
MD61	MD61	AE24	I/O	Frame Buffer Data Bus
MD60	MD60	AD24	I/O	Frame Buffer Data Bus
MD59	MD59	AE25	I/O	Frame Buffer Data Bus
MD58	MD58	AF26	I/O	Frame Buffer Data Bus
MD57	MD57	AD25	I/O	Frame Buffer Data Bus
MD56	MD56	AD26	I/O	Frame Buffer Data Bus
MD55	MD55	U26	I/O	Frame Buffer Data Bus
MD54	MD54	U24	I/O	Frame Buffer Data Bus
MD53	MD53	U25	I/O	Frame Buffer Data Bus
MD52	MD52	V24	I/O	Frame Buffer Data Bus
MD51	MD51	V25	I/O	Frame Buffer Data Bus
MD50	MD50	W24	I/O	Frame Buffer Data Bus
MD49	MD49	Y24	I/O	Frame Buffer Data Bus
MD48	MD48	Y25	I/O	Frame Buffer Data Bus
MD47	MD47	AB24	I/O	Frame Buffer Data Bus

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MD46	MD46	AC26	I/O	Frame Buffer Data Bus
MD45	MD45	AA24	I/O	Frame Buffer Data Bus
MD44	MD44	AB23	I/O	Frame Buffer Data Bus
MD43	MD43	AA23	I/O	Frame Buffer Data Bus
MD42	MD42	AA26	I/O	Frame Buffer Data Bus
MD41	MD41	Y23	I/O	Frame Buffer Data Bus
MD40	MD40	Y26	I/O	Frame Buffer Data Bus
MD39	MD39	AA25	I/O	Frame Buffer Data Bus
MD38	MD38	AB25	I/O	Frame Buffer Data Bus
MD37	MD37	AB26	I/O	Frame Buffer Data Bus
MD36	MD36	AC24	I/O	Frame Buffer Data Bus
MD35	MD35	AC25	I/O	Frame Buffer Data Bus
MD34	MD34	AE26	I/O	Frame Buffer Data Bus
MD33	MD33	AF23	I/O	Frame Buffer Data Bus
MD32	MD32	AD23	I/O	Frame Buffer Data Bus
MD31	MD31	A25	I/O	Frame Buffer Data Bus
MD30	MD30	C25	I/O	Frame Buffer Data Bus
MD29	MD29	D24	I/O	Frame Buffer Data Bus
MD28	MD28	E26	I/O	Frame Buffer Data Bus
MD27	MD27	E24	I/O	Frame Buffer Data Bus
MD26	MD26	G26	I/O	Frame Buffer Data Bus
MD25	MD25	H25	I/O	Frame Buffer Data Bus
MD24	MD24	G24	I/O	Frame Buffer Data Bus
MD23	MD23	H24	I/O	Frame Buffer Data Bus
MD22	MD22	H26	I/O	Frame Buffer Data Bus
MD21	MD21	G25	I/O	Frame Buffer Data Bus
MD20	MD20	F24	I/O	Frame Buffer Data Bus
MD19	MD19	G23	I/O	Frame Buffer Data Bus

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MD18	MD18	F25	I/O	Frame Buffer Data Bus
MD17	MD17	F26	I/O	Frame Buffer Data Bus
MD16	MD16	F23	I/O	Frame Buffer Data Bus
MD15	MD15	J25	I/O	Frame Buffer Data Bus
MD14	MD14	K24	I/O	Frame Buffer Data Bus
MD13	MD13	L23	I/O	Frame Buffer Data Bus
MD12	MD12	L24	I/O	Frame Buffer Data Bus
MD11	MD11	M23	I/O	Frame Buffer Data Bus
MD10	MD10	M24	I/O	Frame Buffer Data Bus
MD9	MD9	N25	I/O	Frame Buffer Data Bus
MD8	MD8	N24	I/O	Frame Buffer Data Bus
MD7	MD7	E23	I/O	Frame Buffer Data Bus
MD6	MD6	E25	I/O	Frame Buffer Data Bus
MD5	MD5	D26	I/O	Frame Buffer Data Bus
MD4	MD4	D25	I/O	Frame Buffer Data Bus
MD3	MD3	A26	I/O	Frame Buffer Data Bus
MD2	MD2	C24	I/O	Frame Buffer Data Bus
MD1	MD1	B26	I/O	Frame Buffer Data Bus
MD0	MD0	C26	I/O	Frame Buffer Data Bus
MDM15	MDM15	AE4	Output	Frame Buffer Data Bus Mask
MDM14	MDM14	AF9	Output	Frame Buffer Data Bus Mask
MDM13	MDM13	AF4	Output	Frame Buffer Data Bus Mask
MDM12	MDM12	AD11	Output	Frame Buffer Data Bus Mask
MDM11	MDM11	AF10	Output	Frame Buffer Data Bus Mask
MDM10	MDM10	AD15	Output	Frame Buffer Data Bus Mask
MDM9	MDM9	AE11	Output	Frame Buffer Data Bus Mask
MDM8	MDM8	AE15	Output	Frame Buffer Data Bus Mask
MDM7	MDM7	W26	Output	Frame Buffer Data Bus Mask

Table 3.5 Frame Buffer Memory Signals (Continued)

Name	Abbr. Name	Position	Type	Description
MDM6	MDM6	R24	Output	Frame Buffer Data Bus Mask
MDM5	MDM5	W25	Output	Frame Buffer Data Bus Mask
MDM4	MDM4	T24	Output	Frame Buffer Data Bus Mask
MDM3	MDM3	P24	Output	Frame Buffer Data Bus Mask
MDM2	MDM2	J26	Output	Frame Buffer Data Bus Mask
MDM1	MDM1	R25	Output	Frame Buffer Data Bus Mask
MDM0	MDM0	J23	Output	Frame Buffer Data Bus Mask
MDSF_A	MDSFA	T26	Output	Frame Buffer A Special Function
MSDF_B	MDSFB	AF6	Output	Frame Buffer B Special Function
MRAS_A	MRASA	K25	Output	Frame Buffer Port A RAS
MRAS_B	MRASB	AD14	Output	Frame Buffer Port B RAS
MWE_A	MWEA	J24	Output	Frame Buffer Port A Write Enable
MWE_B	MWEB	AD13	Output	Frame Buffer Port B Write Enable

Table 3.6 Monitor Signals

Name	Abbr. Name	Position	Type	Description
BLUE	BLUE	B12	Output	DAC Analog Blue
DAC_RSET	DRSET	B11	Wire	DAC Full Scale Set
GREEN	GREEN	A12	Output	DAC Analog Green
HSYNC	HSYNC	A3	Output	Horizontal Sync to Monitor
RED	RED	D12	Output	DAC Analog Red
VSYNC	VSYNC	A1	Output	Vertical Sync to Monitor

Table 3.7 VMI Interface Signals

Name	Abbr. Name	Position	Type	Description
VMI_BLANK	VBLNK	C14	I/O	External VMI Blank Signal
VMI_CS_N	VCS	A9	I/O	External VMI Chip Select
VMI_DS_N	VDS	B8	I/O	External VMI Data Strobe
VMI_HA3	VHA3	B9	Output	VMI Host Port Address Bus
VMI_HA2	VHA2	B13	Output	VMI Host Port Address Bus
VMI_HA1	VHA1	C12	Output	VMI Host Port Address Bus
VMI_HA0	VHA0	A14	Output	VMI Host Port Address Bus
VMI_HD7	VHD7	D6	I/O	VMI Host Port Data Bus
VMI_HD6	VHD6	C6	I/O	VMI Host Port Data Bus
VMI_HD5	VHD5	D7	I/O	VMI Host Port Data Bus
VMI_HD4	VHD4	C7	I/O	VMI Host Port Data Bus
VMI_HD3	VHD3	C8	I/O	VMI Host Port Data Bus
VMI_HD2	VHD2	D9	I/O	VMI Host Port Data Bus
VMI_HD1	VHD1	C9	I/O	VMI Host Port Data Bus
VMI_HD0	VHD0	A10	I/O	VMI Host Port Data Bus
VMI_HSYNC	VHSYNC	D14	I/O	VMI Horizontal Sync
VMI_INT_N	VINT	A6	I/O	VMI Interrupt
VMI_PCLK	VPCLK	C13	I/O	VMI Pixel Clock
VMI_PD7	VPD7	B15	I/O	VMI Pixel Bus
VMI_PD6	VPD6	A15	I/O	VMI Pixel Bus
VMI_PD5	VPD5	D16	I/O	VMI Pixel Bus
VMI_PD4	VPD4	C15	I/O	VMI Pixel Bus
VMI_PD3	VPD3	B16	I/O	VMI Pixel Bus
VMI_PD2	VPD2	A16	I/O	VMI Pixel Bus
VMI_PD1	VPD1	A17	I/O	VMI Pixel Bus
VMI_PD0	VPD0	C16	I/O	VMI Pixel Bus
VMI_RDY_N	VRDY	A7	I/O	VMI Ready

Table 3.7 VMI Interface Signals (Continued)

Name	Abbr. Name	Position	Type	Description
VMI_RESET_N	VRST	B7	I/O	VMI Reset
VMI_RW_N	VRW	A8	I/O	VMI Host Port Read/Write
VMI_VSYNC	VVSYNC	B14	I/O	VMI Vertical Sync

Table 3.8 Digital RGB Interface Signals

Name	Abbr. Name	Position	Type	Description
TV_BLANK	TBLNK	A20	I/O	Digital RGB Blank
TV_CLK_OUT	TCLKO	B20	I/O	Digital RGB Clock Out
TV_DATA11	TVD11	B21	IO	Digital RGB Data Bus
TV_DATA10	TVD10	C21	IO	Digital RGB Data Bus
TV_DATA9	TVD9	D22	IO	Digital RGB Data Bus
TV_DATA8	TVD8	A22	IO	Digital RGB Data Bus
TV_DATA7	TVD7	B22	IO	Digital RGB Data Bus
TV_DATA6	TVD6	C22	IO	Digital RGB Data Bus
TV_DATA5	TVD5	A23	IO	Digital RGB Data Bus
TV_DATA4	TVD4	B23	IO	Digital RGB Data Bus
TV_DATA3	TVD3	C23	IO	Digital RGB Data Bus
TV_DATA2	TVD2	B24	IO	Digital RGB Data Bus
TV_DATA1	TVD1	A24	IO	Digital RGB Data Bus
TV_DATA0	TVD0	B25	IO	Digital RGB Data Bus
TV_HSYNC	THSYNC	A21	I/O	Digital RGB HSYNC
TV_INCLK	TICLK	D20	Input	Digital RGB Clock In
TV_RESET	TRST	C20	I/O	Digital RGB Reset
TV_VSYNC	TVSYNC	D21	I/O	Digital RGB VSYNC

Table 3.9 Miscellaneous Pins

Name	Abbr. Name	Position	Type	Description
CLK_OUT	CLKO	D13	Output	Clock Out
GPIO_2	GPIO2	C4	Input	General Purpose I/O Bus
GPIO_1	GPIO1	B4	Output	General Purpose I/O Bus
GPIO_0	GPIO0	A4	I/O	General Purpose I/O Bus
ROM_CS_N	ROMCS	B6	Output	ROM Chip Select
ROM_OE_N	ROMOE	A5	Output	ROM Output Enable
ROM_WE_N	ROMWE	C5	Output	ROM Write Enable
SDA1	SDA1	D5	I/O	VMI (Feature Connector)
SDA0	SDA0	B3	I/O	DDC (Monitor Connector)
SDC1	SCK1	B5	I/O	VMI (Feature Connector)
SDC0	SCK0	C3	I/O	DDC (Monitor Connector)
XIN	XIN	A19	Analog	Crystal In
XOUT	XOUT	C18	Analog	Crystal Out
	Unused	AE13	Unused	No Connect

Table 3.10 Power and Ground Pins

Name	Abbr. Name	Position	Type	Description
AGP_PLL_VDD	APVDD	D18	Power	AGP_PLL Power
AGP_PLL_VSS	APVSS	C17	Ground	AGP_PLL Ground
DAC_AVDD	DAVDD	D11	Power	DAC Power
DAC_AVDD_I	DAVDDI	C11	Power	DAC Power
DAC_AVSS	DAVSS	A11	Ground	DAC Ground
DAC_AVSS_R	DVSSR	B10	Ground	DAC Ground
GND12	GND	D10	Ground	Digital Ground
GND11	GND	D17	Ground	Digital Ground
GND10	GND	D23	Ground	Digital Ground
GND9	GND	K23	Ground	Digital Ground
GND8	GND	U23	Ground	Digital Ground
GND7	GND	AC23	Ground	Digital Ground
GND6	GND	AC17	Ground	Digital Ground
GND5	GND	AC10	Ground	Digital Ground
GND4	GND	AC4	Ground	Digital Ground
GND3	GND	U4	Ground	Digital Ground
GND2	GND	K4	Ground	Digital Ground
GND1	GND	D4	Ground	Digital Ground
IDDQ	IDDQ	A2		
PLL_AVDD1	PAVDD1	C19	Power	Phase Locked Loop Power
PLL_AVDD0	PAVDD0	B18	Power	Phase Locked Loop Power
PLL_AVSS1	PAVSS1	B19	Ground	Phase Locked Loop Ground
PLL_AVSS0	PAVSS0	A18	Ground	Phase Locked Loop Ground
Thermal Balls	T_BALL	J:V 18:9	Ground	Thermal Control (100 pins)
VBG	VBG	C10		
VCC8	VCC	D8	Power	Digital Power
VCC7	VCC	D19	Power	Digital Power

Table 3.10 Power and Ground Pins (Continued)

Name	Abbr. Name	Position	Type	Description
VCC6	VCC	H23	Power	Digital Power
VCC5	VCC	W23	Power	Digital Power
VCC4	VCC	AC19	Power	Digital Power
VCC3	VCC	AC8	Power	Digital Power
VCC2	VCC	W4	Power	Digital Power
VCC1	VCC	H4	Power	Digital Power
VCC_CORE9	VCC_C	P26	Power	Digital Power
VCC_CORE8	VCC_C	A13	Power	Digital Power
VCC_CORE7	VCC_C	D15	Power	Digital Power
VCC_CORE6	VCC_C	T25	Power	Digital Power
VCC_CORE5	VCC_C	AF14	Power	Digital Power
VCC_CORE4	VCC_C	AD12	Power	Digital Power
VCC_CORE3	VCC_C	U3	Power	Digital Power
VCC_CORE2	VCC_C	P1	Power	Digital Power
VCC_CORE1	VCC_C	N3	Power	Digital Power

3.4 Pin Descriptions

The following sections are the detailed, formal pin descriptions. These descriptions are organized exactly the same as the tables.

3.4.1 PCI Interface

The pins on the PCI interface connect directly to the corresponding pins on the PCI bus. These pins are organized so that short, direct traces can be run to the connector.

Name	Description
PCI_AD[31:0]	**PCI Address and Data:** This multiplexed, bidirectional bus transfers address and data during any memory or I/O transaction. The address is on the bus during the clock phase in which PCI_FRAME is active. For I/O, this is a byte address; for configuration and memory transactions, this is a DWORD address. During the data phase(s), PCI_AD[7:0] contain the least significant byte and PCI_AD[31:24] contain the most significant byte. Write data is stable and valid when PCI_IRDY_N is asserted and read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks in which both PCI_IRDY_N and PCI_TRDY_N are asserted.
PCI_CBE[3:0]	**PCI Bus Command and Byte Enables:** These multiplexed pins transfer the bus command and byte enables for any transaction. During the address phase, these pins are driven by the initiator with the bus command. During data phase(s) these pins are used as byte enables. Byte Enables are valid for the entire data cycle and specify the byte lanes that carry meaningful data. PCI_CBE0 is associated with PCI_AD[7:0]; PCI_CBE3 is associated with PCI_AD[31:24].
PCI_CLK	**PCI Clock:** The clock provides timing for all transactions on PCI. All PCI timing is defined with respect to the rising edge of this clock. Voodoo3 supports 66 MHz PCI Clock.
PCI_DEVSEL	**PCI Bus Device Select:** When a device drives this signal active, it indicates the device has decoded the address on the bus as belonging to itself. This signal is a sustained Tri-State output as defined in the PCI specification.
PCI_FRAME	**PCI Bus Cycle Frame:** This signal is driven by the initiator to indicate the beginning and duration of an access. PCI_FRAME is asserted to indicate a bus transaction is beginning. While PCI_FRAME is active, data transfers continue. When PCI_FRAME is deasserted, the transaction is in the final data phase.
PCI_GNT_N	**PCI Bus Grant:** This input indicates to the agent that bus access is granted. This is a point-to-point signal; each master has its own GNT. This pin is used without PCI bus request (REQ#) for AGP mastership.
PCI_IDSEL	**PCI Bus Initialization Device Select:** This input is a chip select in lieu of the upper 24 address lines during configuration read and write cycles. This signal is replaced with AD16 when Voodoo3 is configured for AGP.

3.4.1 PCI Interface *(cont)*

Name	Description
PCI_INTA_N	**PCI Bus Interrupt Request:** This open-collector output is driven low when Voodoo3 is requesting an interrupt. This pin is always connected to INTA#.
PCI_IRDY_N	**PCI Bus Initiator Ready:** This active-low signal indicates the initiating agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock during which both PCI_IRDY_N and PCI_TRDY_N are sampled active. During a write, PCI_IRDY_N indicates that valid data is present on PCI_AD[31:0]. During a read, PCI_IRDY_N indicates the bus master is ready to accept data. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.
PCI_PAR	**PCI Bus Parity:** This signal provides even parity across PCI_AD[31:0] and PCI_CBE[3:0]. Parity generation is required for all PCI agents. Voodoo3 does not check parity.
PCI_RESET_N	**PCI Reset:** This active-low signal initializes the Voodoo3 to a known state. On the rising edge of PCI_RESET_N, the chip reads configuration information from the VMI address and data buses. See Chapter 4. Also, subsystem and subsystem vendor information is loaded from four bytes of the ROM into PCI2C. See the description of PCI2C in the SW Programming Guide.
PCI_STOP_N	**PCI Bus Stop Request:** This active-low signal indicates the target is requesting the master to stop the current transaction. This signal is a sustained Tri-State output as defined in the PCI specification.
PCI_TRDY_N	**PCI Bus Target Ready:** This active-low signal indicates the target's ability to complete the current data phase of the transaction. A data phase is completed on any clock during which both PCI_IRDY_N and PCI_TRDY_N are sampled active. During a write, PCI_TRDY_N indicates that the target is ready to accept data. During a read, PCI_TRDY_N indicates valid data is present on PCI_AD[31:0]. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together. This signal is a sustained Tri-State output as defined in the PCI specification.

3.4.2 AGP Interface

The pins on the AGP interface connect directly to the corresponding pins on the AGP bus. These pins are organized so that short, direct traces can be run to the connector.

Name	Description
AGP_AD_STB1	**AGP AD Bus Strobe 1:** This input provides timing for 2X data transfer mode on AD[31:16].
AGP_AD_STB0	**AGP AD Bus Strobe 2:** This input provides timing for 4X data transfer mode on AD[15:0].
AGP_RBF_N	**AGP Bus Read Buffer Full:** When this active-low output is asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.
AGP_SB_STB:	**AGP Sideband Strobe:** This output provides timing for SBA[7:0] and is always driven by the AGP master. When the Sideband Strobes have been idle, a synchronization cycle must be performed before a request can be enqueued.
AGP_SBA[7:0]	**AGP Bus Sideband Address Port:** This bus provides an additional bus to pass address and command from the master to the target.
AGP_ST[2:0]	**AGP Bus Status:** This bus provides information from the arbiter to the Voodoo3 on what it may do. This bus has meaning only when PCI_GNT_N is asserted.
AGP_VREF	**AGP Voltage Reference:** This input supplies the switching threshold for the AGP receivers. This input is derived from VDDQ3.3 on the AGP interface through a voltage divider network. See the schematic diagram of the reference design.

3.4.3 Frame Buffer Memory

This group of pins provide the interface to the SGRAM/SDRAM frame buffer. The A and B ports connect to the SGRAM/SDRAMs providing MD[63:0] and MD[127:64], respectively. Doubling up on control lines reduces the loading and makes for a tighter layout. MCS0 and MCS1 connect to two banks of four devices each.

Name **Description**

MA_A[10:0] **Memory Address A Bus:** This multiplexed bus supplies the address to the SGRAM/SDRAMs providing MD[63:0].
The exact connections of the MA lines to the SGRAM/SDRAM inputs depends on the memory devices, as detailed in the table. The device pin names in this table are Samsung nomenclature.

Pin	8 Mbit SGRAM	16 Mbit SGRAM	16 Mbit SDRAM
MA_A/B[8:0]	A[8:0]	A[8:0]	A[8:0]
MA_A/B[9]	n/c (BA1 on 16 Mbit)	BA1	A[9]
MA_A/B[10]	BA0 (band address)	BA1	BA
MCS_0	Bank Select		A10 (MD[127:64])
MCS_1			A10 (MD[63:0])

MA_B[10:0] **Memory Address B Bus:** This multiplexed bus supplies the address to the SGRAM/SDRAMs providing MD[127:64].

MCAS_A **Memory Column Address Strobe A:** This signal supplies CAS to the SGRAM/SDRAMs providing MD[63:0].

MCAS_B **Memory Column Address Strobe B:** This signal supplies CAS to the SGRAM/SDRAMs providing MD[127:64].

MCLKA **Memory Clock A:** This signal supplies the clock to the SGRAM/SDRAMs providing MD[63:0]. This signal requires one series termination resistor placed as close to the pin as possible for each SGRAM/SDRAM. The evaluation board uses 0 ohms. In addition, this pin drives MCLKA_IN. This minimizes clock skew when the SGRAM/SDRAMs are supplying data to Voodoo3.

MCLKA_IN **Memory Clock A Feedback:** This input supplies the clock which latches read data from the SGRAM/SDRAMs providing MD[63:0]. This input must be driven from MCLKA.

3.4.3 Frame Buffer Memory *(cont)*

Pin	Description
MCLKB	**Memory Clock B:** This signal supplies the clock to the SGRAM/SDRAMs providing MD[127:64]. This signal requires one series termination resistor placed as close to the pin as possible for each SGRAM/SDRAM. The evaluation board uses 0 ohms. In addition, this output drives MCLKB_IN. This minimizes clock skew when the SGRAM/SDRAMs are supplying data to Voodoo3.
MCLKB_IN	**Memory Clock B Feedback:** This input supplies the clock which latches read data from the SGRAM/SDRAMs providing MD[127:64]. This input must be driven from MCLKB.
MCS_0	**Memory Chip Select 0:** This output connects to the first bank of four SGRAM/SDRAMs.
MCS_1	**Memory Chip Select 1:** This output connects to an optional second bank of SGRAMs. This pin is not used if the array is SDRAMs.
MD[127:0]	**Memory Data Bus:** This is a 128-bit bidirectional data bus. The evaluation board uses the following connections for the first bank. The connections to the second bank are the same except they use MCS_1.
MDM[15:0]	**Frame Buffer Data Mask:** This bus provides the byte-write mask for the 128-bit data.
MDSF_A	**Frame Buffer Special Function A:** This pin supplies the special function control for the SGRAMs providing MD[63:0]. This is a no-connect in a SDRAM array.
MDSF_B	**Frame Buffer Special Function B:** This pin supplies the special function control for the SGRAMs providing MD[127:64]. This is no-connect in a SDRAM array.
MRAS_A	**Frame Buffer Row Address Strobe A:** This pin supplies RAS for the SGRAM/SDRAMs providing MD[63:0].
MRAS_B	**Frame Buffer Row Address Strobe B:** This pin supplies RAS for the SGRAM/SDRAMs providing MD[127:64].
MWE_A	**Frame Buffer Write Enable A:** This pin supplies write enable for the SGRAM/SDRAMs providing MD[63:0].
MWE_B	**Frame Buffer Write Enable B:** This pin supplies write enable for the SGRAM/SDRAMs providing MD[127:64].

Device:	U1	U2	U3	U4
MD	[31:0]	[63:32]	[95:64]	[127:96]
MDM	[3:0]	[7:4]	[11:8]	[15:12]
Controls, Address	A	A	B	B
Chip Select	0	0	0	0

3.4.4 Monitor

These pins are the monitor interface.

Bit	Description
BLUE	**Pixel Blue Content:** This analog output supplies current corresponding to the blue content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
DAC_RSET	**Video DAC RSET:** This pin is used to set the full scale DAC output current. A resistor must be connected between this pin and DAV_VSS. On the evaluation board, this is 56.2 ohms, 1% tolerance.
GREEN	**Pixel Green Content:** This analog output supplies current corresponding to the green content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
HSYNC	**Horizontal Sync:** This output supplies horizontal sync to the monitor. This output should have a series termination resistor placed as close to the pin as possible. The evaluation board uses 47 ohms. The evaluation board has a low-pass filter consisting of a bead and 100 pF capacitor close to the DB-15 connector.
RED	**Pixel Red Content:** This analog output supplies current corresponding to the red content of the pixel being refreshed. This output should have a 75 ohm resistor returned to DAC_VSS placed as close to the pin as possible. The monitor should supply a 75 ohm parallel termination for a net impedance of 37.5 ohms. The evaluation board has surge suppression diodes to VCC and ground and a low-pass filter consisting of a bead and 22 pF capacitor close to the DB-15 connector.
VSYNC	**Vertical Sync:** This output supplies vertical sync to the monitor. This output should have a series termination resistor placed as close to the pin as possible. The evaluation board uses 47 ohms. The evaluation board has a low-pass filter consisting of a bead and 100 pF capacitor close to the DB-15 connector.

3.4.5 VMI Interface

Bit	Description
VMI_BLANK	**VMI VACTIVE:** This input indicates that valid pixel data is being transmitted on VMI_PD[7:0]. Although transitions in VACTIVE are allowed to support common HREF/ VREF systems, VACTIVE is intended to allow a hardware mechanism for cropping data.
VMI_CS_N	**VMI Chip Select:** This output supplies the chip select for the VMI Host interface.
VMI_DS_N	**VMI Data Strobe:** When the VMI interface is configured for mode A, this is an active-low data strobe. When the VMI interface is configured for mode B, this is an active-low read command. This pin also supplies ROM address bit 15.
VMI_HA[3:0]	**VMI Host Port Address Bus:** This bus supplies the address for the VMI host interface port. This bus also supplies ROM address bits [11:8].
VMI_HD[7:0]	**VMI Host Port Data Bus:** This bidirectional bus transfers data across the VMI host interface port. This bus is also used as the ROM data bus.
VMI_HSYNC	**VMI HREF:** This input is the horizontal reference from the VMI video port.
VMI_INT_N	**VMI INTREQ#:** This active input is the interrupt request from the VMI interface. This pin also supplies ROM address bit 13.
VMI_PCLK	**VMI PIXCLK:** This input is the pixel clock from the VMI video port.
VMI_PD[7:0]	**VMI YUV Video Data Bus:** This input bus is the pixel data from the VMI video port. This bus is also the low order eight bits of the ROM address bus.
VMI_RDY_N	**VMI DTACK#/READY:** When the VMI interface is configured for mode A, this is active DTACK# (extend transaction). When the VMI interface is configured for mode B, this is active high READY. This pin also supplies ROM address bit 12.
VMI_RESET_N	**VMI RESET:** This active low signal resets the VMI interface and/or devices to a known condition.
VMI_RW_N	**VMI R/W# WR#:** When the VMI interface is configured for mode A, this is the read/write indicator. When the VMI interface is configured for mode B, this is an active low write command. This pin also supplies ROM address bit 14.
VMI_VSYNC	**VMI VREF:** This input is the vertical reference from the VMI video port.

3.4.6 Digital RGB Interface Signals

This interface supplies digital RGB. It is typically used to drive an LCD encoder or TV encoder, but could be used for any other application requiring digital RGB.

Pin	Description
TV_BLANK	**TV_BLANK_N:** This active low output is the blank signal for the digital RGB out port.
TV_CLK_OUT	**TV Clock Out:** This output supplies the clock for the digital RGB out port.
TV_DATA[11:0]	**TV Data Out:** This 12-bit bus supplies digital RGB data for the digital RGB out port.
TV_HSYNC	**TV_HSYNC:** This pin supplies horizontal sync for the digital RGB out port.

3.4.6 Digital RGB Interface Signals *(cont)*

Pin	Description
TV_INCLK	**TV Clock In:** This input is the clock for the digital RGB out port for slave mode.
TV_RESET	**TV_RESET_N:** This is a reset for the digital RGB out port.
TV_VSYNC	**TV_VSYNC:** This pin supplies vertical sync for the digital RGB out port.

3.4.7 Miscellaneous Pins

The following pins didn't fall into any of the other groups.

Pin	Description
CLK_OUT	**Clock Out:** This clock is used for testing. This is brought to a test point on the reference design but is otherwise not connected.
GPIO_[2:0]	**General Purpose I/O[2:0]:** These pins are dedicated for general purpose I/O. The table indicates how they are assigned on the evaluation board.

Name	Pin	Signal Label	Purpose
GPIO_2	C4	GPIO_2_RD	INSERT# (Z19) on VMI host connector
GPIO_1	B4	No connect	-
GPIO_0[a]	A4	ROM_ACTIVE	Controls BE on analog switch chip (U3)

a. This pin is active (high) when the ROM is accessed (PCI10 + 0x00A0 xxxx).

ROM_CS_N	**ROM Chip Select:** This output connects to the CE pin of the ROM.
ROM_OE_N	**ROM Output Enable:** This output connects to the OE pin of the ROM. This pin is active with ROM_CS_N to read the ROM.
ROM_WE_N	**ROM Write Enable:** This output connects to the WE pin of the ROM. This pin is active with ROM_CS_N for ROM writes (for updating the BIOS).
SDA[1:0]	**Serial Data[1:0]:** These are the data pins of the two I^2C interfaces. SDA1 is used for the feature connector interface, both the TV and xLCD encoders, and the LCD panel connector. SDA0 is used for the CRT monitor (DDC2B) interface.
SDC[1:0]	**Serial Clock[1:0]:** These are the clock pins of the two I^2C interfaces. SDC1 is used for the feature connector interface, both the TV and xLCD encoders, and the LCD panel connector. SDC0 is used for the CRT monitor (DDC2B) interface.
XIN	**Crystal In:** This pin connects to one side of the reference oscillator crystal. No external resistor or capacitors are required. Voodoo3 has internal capacitors. The oscillator is designed for a 18 pF, parallel resonant crystal. 3dfx Interactive, Inc. recommends a tolerance of 50 ppm.

3.4.7 Miscellaneous Pins *(cont)*

Pin	Description
XOUT	**Crystal Out:** This pin connects to one side of the reference oscillator crystal.
Unused	**No Connect:** The following pin is a no connect: AE13

3.4.8 Power and Ground

These are the power and ground pins.

Bit	Description
AGP_PLL_VDD	**AGP_PLL Power:** This pin supplies power to the AGP PLL. This supply is decoupled from V2_5 (2.5V supply) with a bead and then four capacitors: 4.7 uF, 0.1 uF, 0.01 uF, and 0.001 uF. The filters should be close to the pin.
AGP_PLL_VSS	**AGP_PLL Ground Reference:** This pin supplies ground reference to the AGP PLL. It must be connected directly to the ground plane.
DAC_AVDD/I	**DAC Power:** These two pins supply power to the DACs. They are adjacent on the package. This supply is decoupled from V2_5 (2.5V supply) with a bead and then four capacitors: 4.7 uF, 0.1 uF, 0.01 uF, and 0.001 uF. The filters should be close to the pins.
DAC_AVSS/R	**DAC Ground Reference:** These two pins supply ground reference to the DACs. They must be connected directly to the ground plane.
GND[12:1]	**Digital Ground Reference:** These twelve pins supply ground reference to the digital circuitry. Each must be connected directly to the ground plane.
IDDQ	**Output Enable Disable:** This pin must be pulled to VCC.
PLL_AVDD[1:0]	**PLL Power:** These two pins supply power to the PLLs.This supply is decoupled from V2_5 (2.5V supply) with a bead and then four capacitors: 4.7 uF, 0.1 uF, 0.01 uF, and 0.001 uF. The filters should be close to the pins.
PLL_AVSS[1:0]	**PLL Ground Reference:** These two pins supply ground reference to the PLLs.
Thermal	**Thermal Pads:** These 100 pins must be connected directly to the ground plane. They are intended to conduct heat out of the chip onto the PC board. These pins are internally connected to the substrate.
VGB	This pin is not connected on the reference design.
VCC[8:1]	**Digital Power:** These eight pins supply power to the digital circuitry. Each must be connected directly to the power plane. These pins must be well bypassed.
VCC_CORE[9:1]	**Digital Power:** These nine pins supply power to the digital circuitry. Each must be connected directly to the power plane. These pins must be well bypassed.

4 Configuration Options

When PCI_RST goes not active, the levels on VMI_HA[3:0] and VMI_HD[7:0] are loaded into a set of configuration latches. These latches control Voodoo3 behavior. Most of the strapping options can be sensed by software.
To load a zero into a configuration latch, connect a 4700 ohm resistor between the corresponding pin and ground. To load a one into a configuration latch, connect a 4700 ohm resistor between the corresponding pin and 3.3V. Every one of the twelve pins must have a resistor to either power or ground in order to prevent the pin from floating to threshold.

Table 4.1 Strapping Options

Bit	Pin	Description	Level	Readback
11	VMI_HA3	PLL_BYPASS	(used with bit 2)	
10	VMI_HA2	Memory Type	0: SGRAMs 1: SDRAMs	
9	VMI_HA1	SGRAM Init	0: Normal Operation 1: Test Mode	
8	VMI_HA0	IDSEL Select	0: IDSEL (PCI) 1: PCI_AD16 (AGP)	
7	VMI_HD7	Disable PCI IRQ Register	0: Enable 1: Disable	
6	VMI_HD6	SGRAM/SDRAM Size	0: 8 Mbit 1: 16 Mbit	miscInit1[30]
5	VMI_HD5	SGRAM/SDRAM Count	0: 4 Chips 1: 8 Chips	miscInit1[29]
4	VMI_HD4	PCI Device Type	0: VGA 1: Other Multimedia	miscInit1[28]
3	VMI_HD3	AGP Enable	0: Disable 1: Enable	miscInit1[27]
2	VMI_HD2	PCI 66 MHz	0: 33 MHz 1: 66 MHz	miscInit1[26]
1	VMI_HD1	BIOS Size	0: 32K 1: 64K	miscInit1[25]
0	VMI_HD0	DEVSEL Timing	0: Medium 1: Fast	miscInit1[24]

5 Digital RGB Data Formats

Digital RGB data is clocked on both edges of the clock. Which bit is clocked on each edge is controlled by vidInFormat[8].

Table 5.1 Digital RGB Data Formats

Pin	vidInFormat[8] = 0 Chrontel Encoder		vidInFormat[8] = 1 Brooktree Encoder	
	Rising Edge	Falling Edge	Rising Edge	Falling Edge
TV_DATA[11]	G0[4]	R0[7]	R0[7]	G0[4]
TV_DATA[10]	G0[3]	R0[6]	R0[6]	G0[3]
TV_DATA[9]	G0[2]	R0[5]	R0[5]	G0[2]
TV_DATA[8]	B0[7]	R0[4]	R0[4]	B0[7]
TV_DATA[7]	B0[6]	R0[3]	R0[3]	B0[6]
TV_DATA[6]	B0[5]	G0[7]	G0[7]	B0[5]
TV_DATA[5]	B0[4]	G0[6]	G0[6]	B0[4]
TV_DATA[4]	B0[3]	G0[5]	G0[5]	B0[3]
TV_DATA[3]	G0[0]	R0[2]	R0[2]	G0[0]
TV_DATA[2]	B0[2]	R0[1]	R0[1]	B0[2]
TV_DATA[1]	B0[1]	R0[0]	R0[0]	B0[1]
TV_DATA[0]	B0[0]	G0[1]	G0[1]	B0[0]

6 General Purpose I/O

This chapter covers general purpose I/O. There are three pins that are dedicated to general purpose I/O, as shown in Table 6.1.

Table 6.1 Standard GPIO Pins

Name	Pin	Direction	Signal on Eval Board	Register Assignment
GPIO_2	C4	In	GPIO_2_RD	vidSerialParallelPort[30]
GPIO_1	B4	Out	-	vidSerialParallelPort[29]
GPIO_0	A4[a]	I/O	ROM_ACTIVE	

a. This pin is driven active (high) when the ROM is accessed (PCI10 + 0x00A0 xxxx).

7 Serial I/O

There are two serial I/O ports on Voodoo3. Each port comprises two open-drain outputs that can be controlled and sensed with register bits. These ports are similar to I^2C.
By convention, Serial Port 0 is used for DDC (it is wired to the monitor connector).
Serial Port 1 is used for VMI (it is wired to the Feature Connector), the TV encoder and xLCD encoder, and the panel LCD connector.

The following table shows the pin and register bit assignments for the two serial ports.

Table 7.1 Serial I/O Assignments

Signal Name	Pin	vidSerialParallelPort bits		
		Enable	In	Out
SDA1	D5	23	27	25
SDC1	B5	23	26	24
SDA0	B3	18	22	20
SDC0	C3	18	21	19

8 ROM Access

By convention, a graphics adapter card includes a BIOS in a ROM. Twenty-three of the 26 pins needed to access the ROM are multiplexed with VMI pins, as shown in Table 8.1.

Table 8.1 ROM Access Pins

ROM Function	Pin Name	Pin
A15	VMI_DS_N	B8
A14	VMI_RW_N	A8
A13	VMI_INT_N	A6
A12	VMI_RDY_N	A7
A11	VMI_HA3	B9
A10	VMI_HA2	B13
A9	VMI_HA1	C12
A8	VMI_HA0	A14
A7	VMI_PD7	B15
A6	VMI_PD6	A15
A5	VMI_PD5	D16
A4	VMI_PD4	C15
A3	VMI_PD3	B16
A2	VMI_PD2	A16
A1	VMI_PD1	A17
A0	VMI_PD0	C16
D7	VMI_HD7	D6
D6	VMI_HD6	C6
D5	VMI_HD5	D7
D4	VMI_HD4	C7
D3	VMI_HD3	C8
D2	VMI_HD2	D9
D1	VMI_HD1	C9
D0	VMI_HD0	A10

9 DC Specifications

9.1 Absolute Maximum Ratings

Stresses above those listed in Table 9.1 may cause permanent damage to system components. These are stress ratings only and functional operation at these or any conditions outside those indicated in Table 9.2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 9.1 Absolute Maximum Ratings

Symbol	Description	Rating
T_{STG}	Storage Temperature	-40 to 125 degrees C
V_{IN}	Input Voltage on any pin	-0.5 V to V_{CC} + 0.5 V
V_A	Power Supply Voltage	3.60 V
I_{OUT}	DC output current (per pin)	tbd
T_C	Max Case Temperature	105 degrees C
T_J	Max Junction Temperature	125 degrees C[a]

a. For operation at case temperature above 105 degrees C, consult application note. Maximum junction temperature is 125 degrees C under any conditions.

9.2 DC Characteristics and Recommended Operating Conditions

Table 9.2 DC Characteristics and Recommended Operating Conditions

Symbol	Description	Test Conditions	- 250		- 333	
			Min	Max	Min	Max
T_C	Case Temperature	Operating	0 ° C	100° C	0 ° C	100° C
V_{IH}	Input High Voltage	V_{CC} =				
V_{IL}	Input Low Voltage	V_{CC} =	0.0 V	0.8 V	0.0 V	0.8 V
I_{IH}	Input High Current	$V_{IH} = V_{CC}$	-	10 uA	-	10 uA
I_{IL}	Input Low Current	V_{IL} =	-10 uA	-	-10 uA	-
V_{OH}	Output High Voltage	I_{OH} =	0.9 * V_{CC}	-	0.9 * V_{CC}	-
V_{OL}	Output Low Voltage	I_{OL} =	-	0.4 V	-	0.4 V
I_{OL}	Output Leakage Current	$0V \le V_{IN} \le V_{CC}$	-10 uA	10 uA	-10 uA	10 uA

Table 9.2 DC Characteristics and Recommended Operating Conditions

Symbol	Description	Test Conditions	- 250		- 333	
			Min	Max	Min	Max
C_{IN}	Input Capacitance[a]	All except XIN, XOUT	-	10 pF	-	10 pF
C_{INX}	Input Capacitance	XIN, XOUT	tbd	tbd	tbd	tbd
C_{OUT}	Output Capacitance[a]	-	-	10 pF	-	10 pF

a. This is not 100% tested, but is periodically sampled.

9.3 VCC Limits

Table 9.3 Supply Current and Voltage

Device	Test Conditions	I_{core} Typical	I_{IO} Typical	Core VCC (volts)			I/O VCC (volts)		
				Min	Typ	Max	Min	Typ	Max
-250	GRX Clk = 125 MHz Core Vcc = 2.20V I/O Vcc = 3.3V	2.00A	0.35A	2.16	2.20	2.27	3.15	3.30	3.45
-333	GRX Clk = 143 MHz Core Vcc = 2.55V I/O Vcc = 3.3V	2.47A	0.35A	2.50	2.55	2.63	3.15	3.30	3.45
-333	GRX Clk = 166 MHz Core Vcc = 2.69V I/O Vcc = 3.3V	2.94A	0.33A	2.63	2.69	2.77	3.15	3.30	3.45
-XXX	GRX Clk = 183 MHz Core Vcc = 2.76V I/O Vcc = 3.3V	3.20A	0.36A	2.70	2.76	2.84	3.15	3.30	3.45

9.4 Package Thermal Characteristics

Table 9.4 Thermal Characteristics

Parameter	Conditions[a]	- 250	- 333
		Degrees C / watt	Degrees C / watt
θJA	Typical, no heat sink	10.0	n/a
θJA	With heat sink	n/a	6.0

a. See Application Note to determine actual theta JA and junction temperature.

9.5 DAC Characteristics

Table 9.5 DAC Characteristics

Symbol	Parameter	MAX	Units	Conditions	Notes
R	Resolution	8	bits		
IO	Output current	tbd	mA	VO < 1V	
TR	Analog output rise/full time	tbd	ns	10% to 90% full scale	a b
TS	Analog output settling time	tbd	ns	50% FS change to remaining within 2%	a b
TSK	Analog output skew	tbd	ns		a b c d
FDT	DAC-to-DAC correlation	tbd	%		a b c d
GI	Glitch impulse	tbd	pV/sec		b
IL	Integral linearity	tbd	LSB		
DL	Differential linearity	tbd	LSB		b

a. Load is 50 ohms and 30 pF per analog output.
b. RSET = 147 ohms
c. Outputs loaded identically.
d. About the mid-point of the distribution of the three DAC's measured at full-scale output.

10 AC Specifications

In general, these waveforms and tables very closely follow those of the respective specifications.

10.1 Maximum Clock Rates

Table 10.1 shows the maximum rated operational frequencies for Voodoo3.

Table 10.1 Maximum Clock Rates

Clock	Maximum Frequency	
	-250	-333
GRX	125 MHz	166 MHz
MCLK	125 MHz	166 MHz

10.2 Clock Input Timing

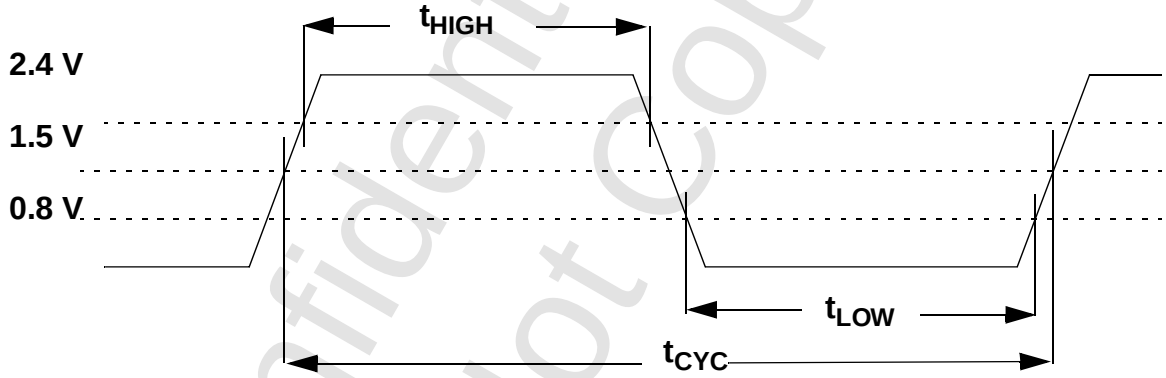


Figure 10.1 Clock Input Waveform

Table 10.2 PCI_CLK Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	15	30	ns
t_{HIGH}	CLK high time	6	-	ns
t_{LOW}	CLK low time	6	-	ns
-	CLK slew rate	1.5	4	V/ns

Table 10.3 VMI_PCLK (VMI Video Capture Mode) Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	35	-	ns

Table 10.4 TV_INCLK (TV out Mode) Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	tbd	tbd	ns
t_{HIGH}	CLK high time	tbd	-	ns
t_{LOW}	CLK low time	tbd	-	ns

Table 10.5 GRX_CLK Timing[a]

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	tbd	tbd	ns
t_{HIGH}	CLK high time	tbd	-	ns
t_{LOW}	CLK low time	tbd	-	ns

a. This clock is used for factory testing. This table is reference only.

10.3 Clock Out Timing

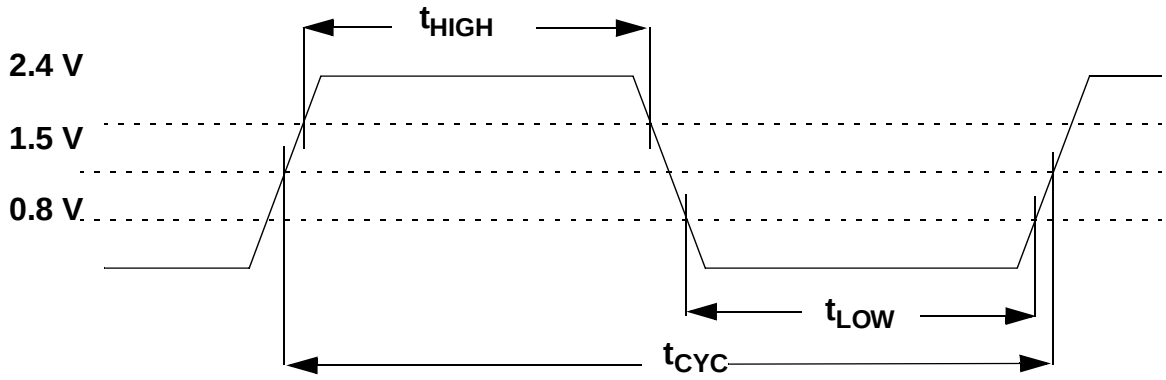


Figure 10.2 Clock Out Waveform

Table 10.6 MCLKA/MCLKB Timing

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	8.6	-	ns
t_{HIGH}	CLK high time	4	-	ns
t_{LOW}	CLK low time	4	-	ns

Table 10.7 TV_CLK_OUT Timing: TV Out Mode

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	10	-	ns
t_{HIGH}	CLK high time	5	-	ns
t_{LOW}	CLK low time	5	-	ns

Table 10.8 TV_CLK_OUT Timing: LCD Out Mode

Symbol	Parameter	Min	Max	Units
t_{CYC}	CLK cycle time	10	-	ns
t_{HIGH}	CLK high time	5	-	ns
t_{LOW}	CLK low time	5	-	ns

10.4 Reset Timing

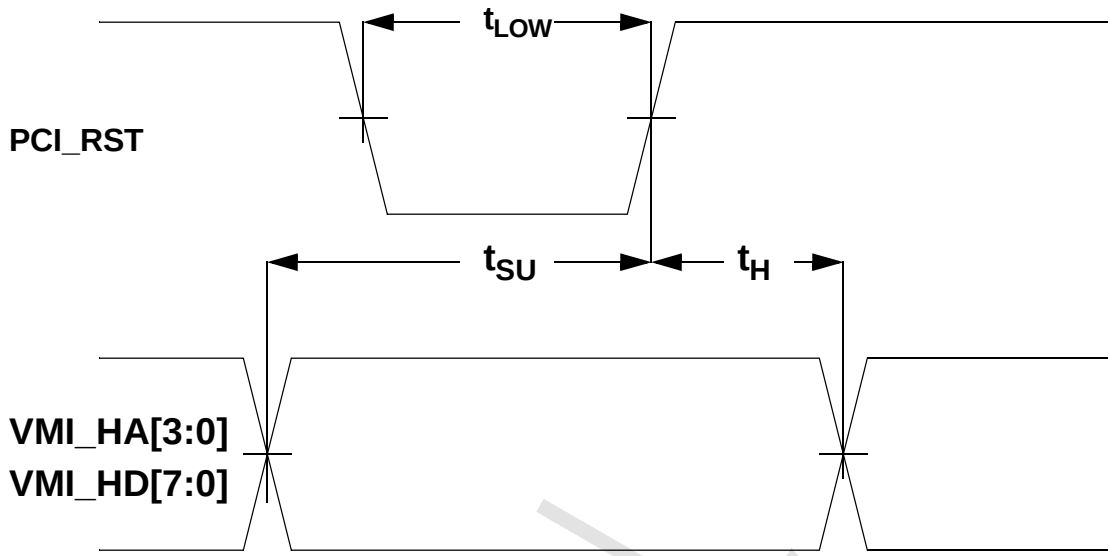


Figure 10.3 Reset Waveforms

Table 10.9 Reset Timing

Symbol	Parameter	Min	Max	Units
t_{LOW}	PCI_RST pulse width	tbd	-	PCI_CLK
t_{SU}	Strapping Resistor Setup	20	-	ns
t_H	Strapping Resistor Hold	20	-	ns

10.5 PCI/AGP Transmitter (output) Timing

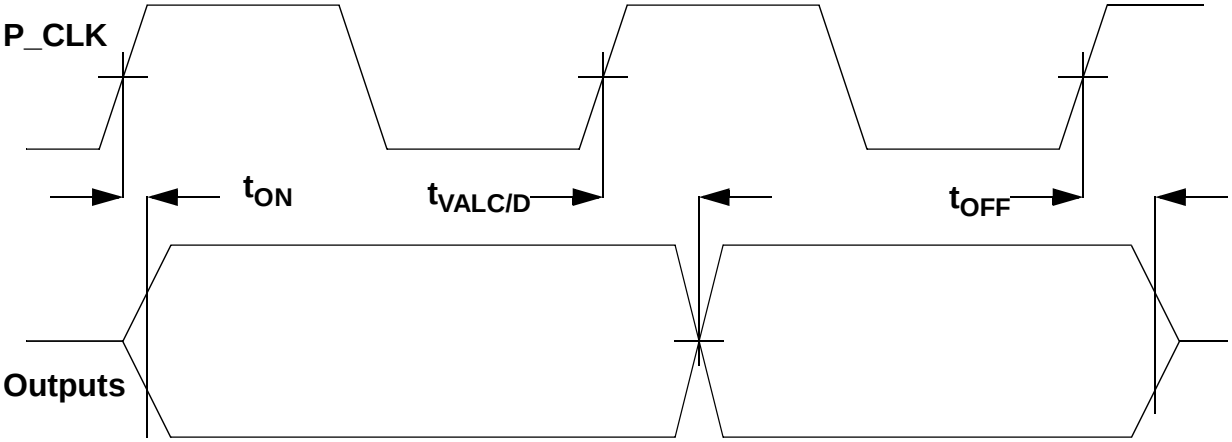


Figure 10.4 PCI/AGP Transmitter Waveforms

Table 10.10 PCI/AGP Transmitter (output) Timing

Symbol	Parameter	Min	Max	Units
t_{ON}	Float to active delay	1.0	6	ns
t_{VALC}	CLK to control signal valid delay	1.0	5.5	ns
t_{VALD}	CLK to data valid delay	1.0	6.0	ns
t_{OFF}	Active to float delay	1	14	ns

10.6 PCI/AGP Receiver (input) Timing

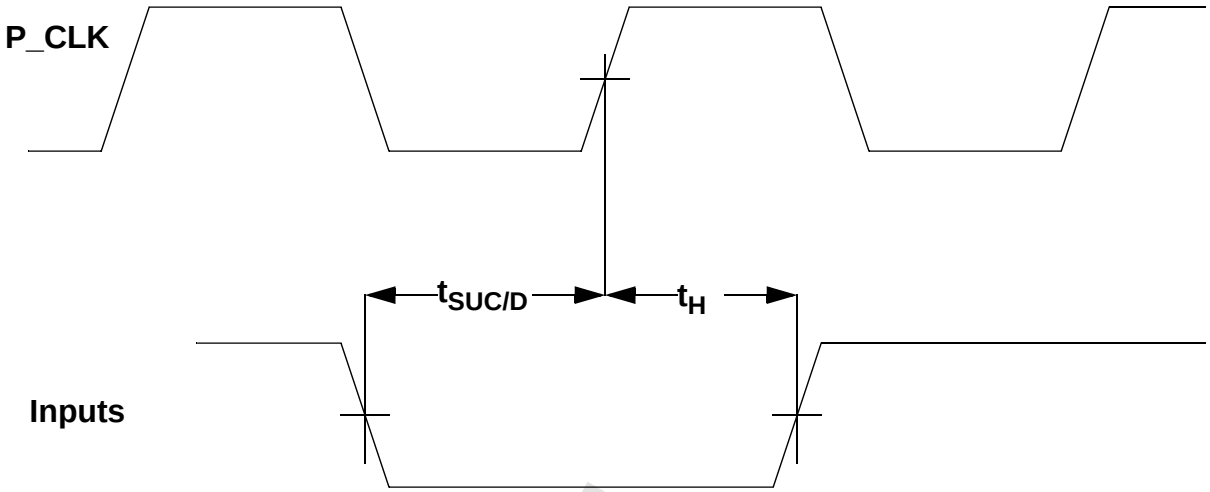


Figure 10.5 PCI/AGP Receiver Waveforms

Table 10.11 PCI/AGP Receiver (input) Timing

Symbol	Parameter	Min	Max	Units
t_{SUC}	Control signals setup time to CLK	6.0	-	ns
t_{SUD}	Data setup time to CLK	5.5	-	ns
t_H	Control signals hold time to CLK	0.0	-	ns

10.7 Frame Buffer Output Timing

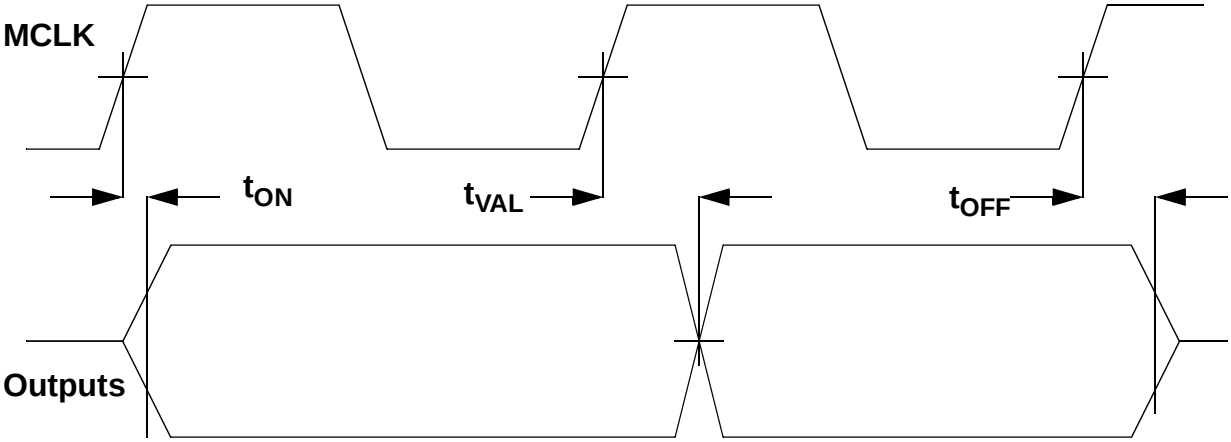


Figure 10.6 Frame Buffer Output Waveforms

Table 10.12 Frame Buffer Output Timing[a]

Symbol	Parameter	Min	Max	Units
t_{ON}	Float to active delay (MD[127:0])	tbd	tbd	ns
t_{VAL}	CLK to control signal valid delay	-	tbd	ns
t_{VAL}	CLK to address valid delay	-	tbd	ns
t_{VAL}	CLK to MD valid delay	-	tbd	ns
t_{OFF}	Active to float delay (MD[127:0])	tbd	tbd	ns

a. 115 MHz MCLK, standard BIOS programming.

10.8 Frame Buffer Input Timing

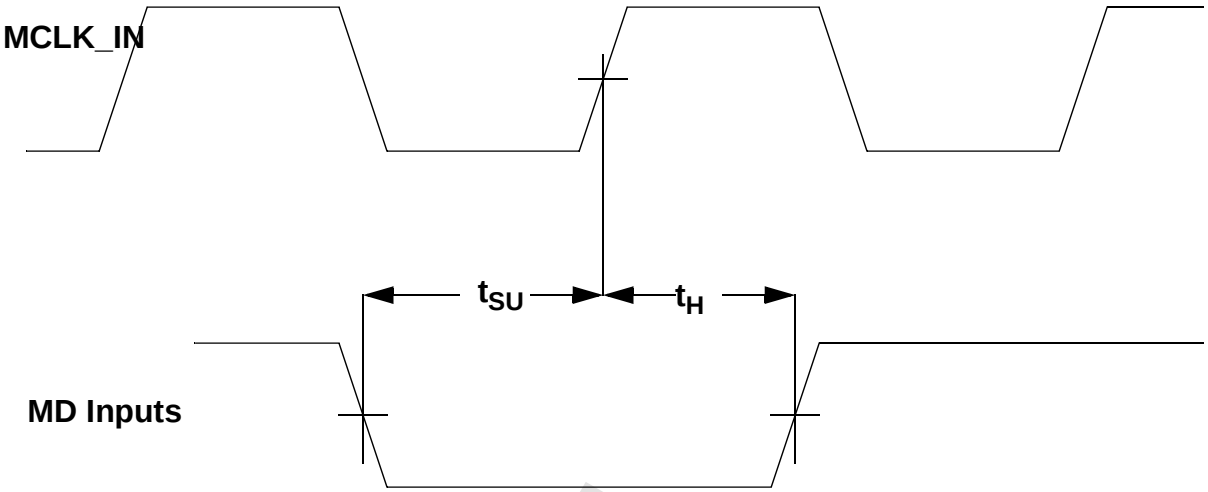


Figure 10.7 Frame Buffer Input Waveforms

Table 10.13 Frame Buffer Input Timing[a]

Symbol	Parameter	Min	Max	Units
t_{SU}	MD setup time to MCLK_IN	tbd	-	ns
t_H	MD hold time to MCLK_IN	tbd	-	ns

a. 115 MHz, standard BIOS programming

10.9 VMI Host Interface Mode A Timing

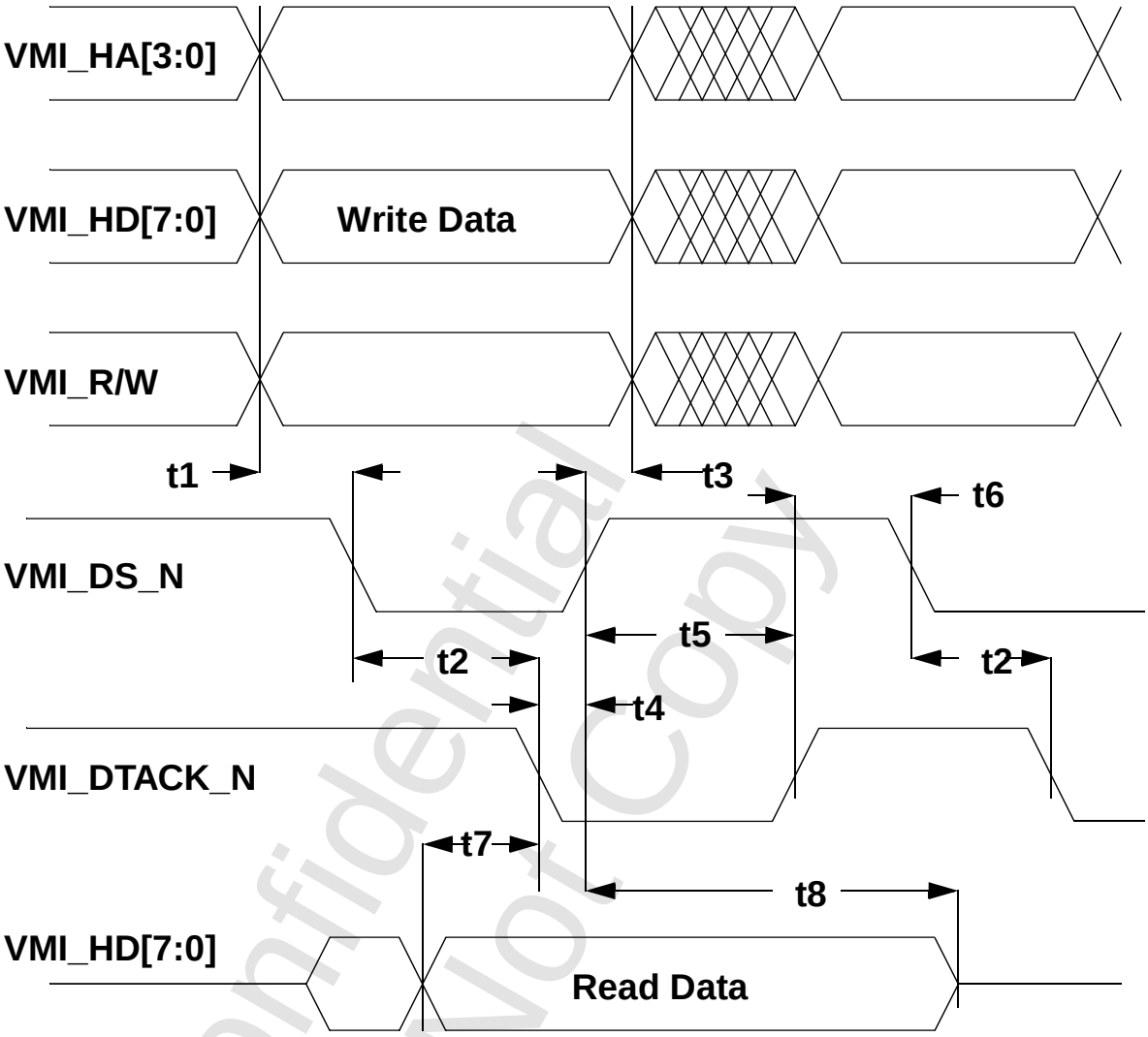


Figure 10.8 VMI Host Interface Mode A Waveforms

Table 10.14 VMI Host Interface Mode A Timing [a]

Symbol	Parameter	Min	Max	Units
t1	HA, HD, R/W# setup to DS# low	5	-	ns
t2	Delay DTACK# low after DS# low	0	13000	ns
t3	HA, HD R/W# hold after DS# high	5	-	ns
t4	Delay DS# high after DTACK# low	5	-	ns

Table 10.14 VMI Host Interface Mode A Timing (Continued)[a]

Symbol	Parameter	Min	Max	Units
t5	Delay DTACK# high after DS# high	0	52	ns
t6	Delay DS# low (next cycle) after DTACK# high	5	-	ns
t7	(Read cycle) HD setup until DTACK# low	10	-	ns
t8	(Read cycle) HD hold after DS# high	0	-	ns

a. The timing parameters of VMI interface host cycles are explicitly controlled by bits in the vidSerialParallelPort register. The timing diagrams and tables are from the VMI specification and are included here for convenience.

10.10 VMI Host Interface Mode B Timing

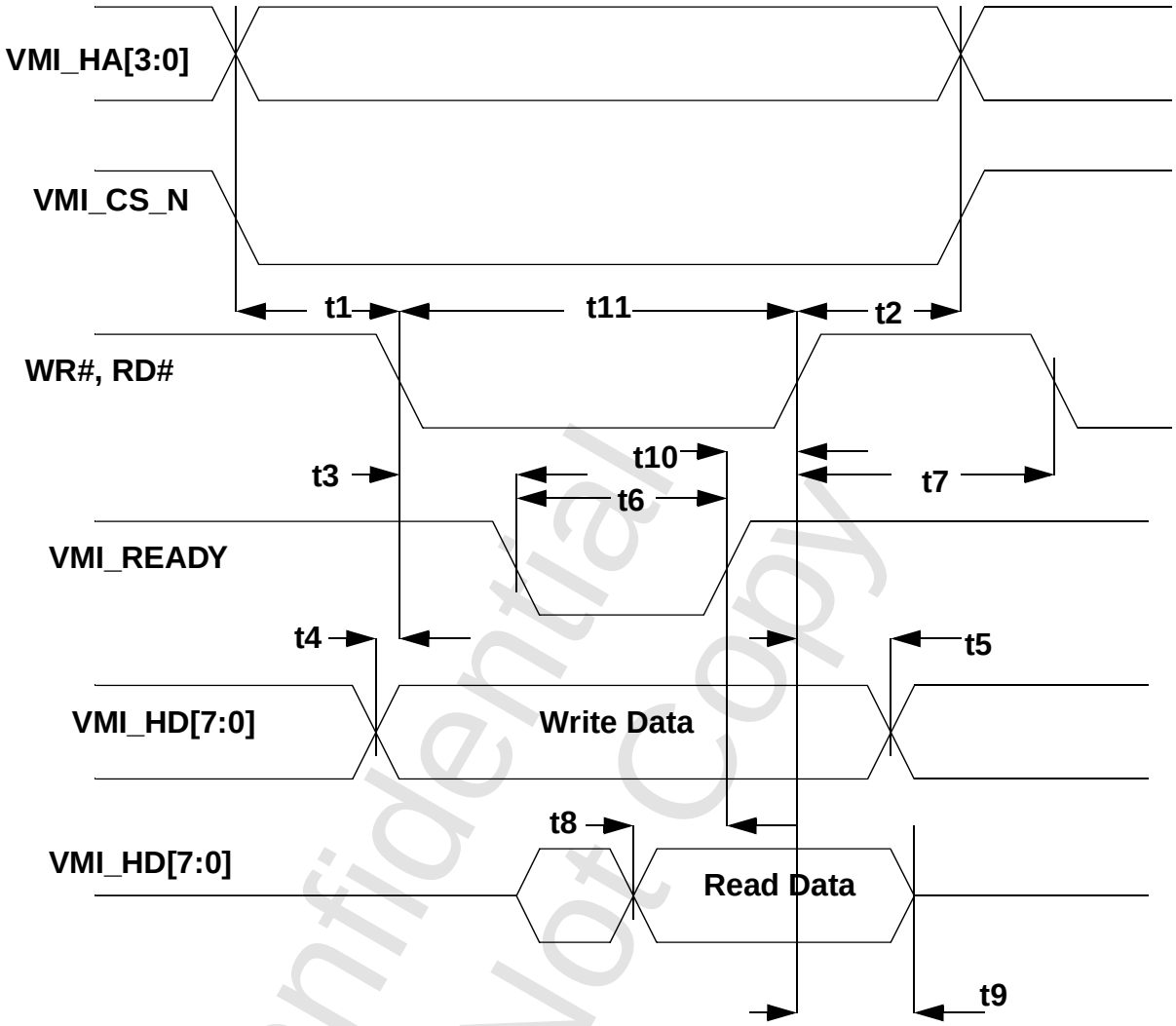


Figure 10.9 VMI Host Interface Mode B Waveforms

Table 10.15 VMI Host Interface Mode B Timing [a]

Symbol	Parameter	Min	Max	Units
t1	HA, CS# setup until WR# or RD# low	10	-	ns
t2	HA, CS# hold after WR# or RD# high	0	-	ns
t3	Delay READY low after WR# or RD# low	-	28	ns
t4	HD setup until WR# low (write cycle)	5	-	ns
t5	HD hold after WR# high (write cycle	10	-	ns

Table 10.15 VMI Host Interface Mode B Timing (Continued)[a]

Symbol	Parameter	Min	Max	Units
t6	READY pulse width	0	-	ns
t7	WR# high until any command	38	-	ns
t8	HD setup until READY active (read cycle)	0	-	ns
t9	HD hold after RD# inactive (read cycle)	0	15	ns
t10	Delay WR# or RD# high after READY high	0	100	ns
t11	Read/Write command pulse width	40	-	ns

a. The timing parameters of VMI interface host cycles are explicitly controlled by bits in the vidSerialParallelPort register. The timing diagrams and tables are from the VMI specification and are included here for convenience.

10.11 VMI Video In Timing

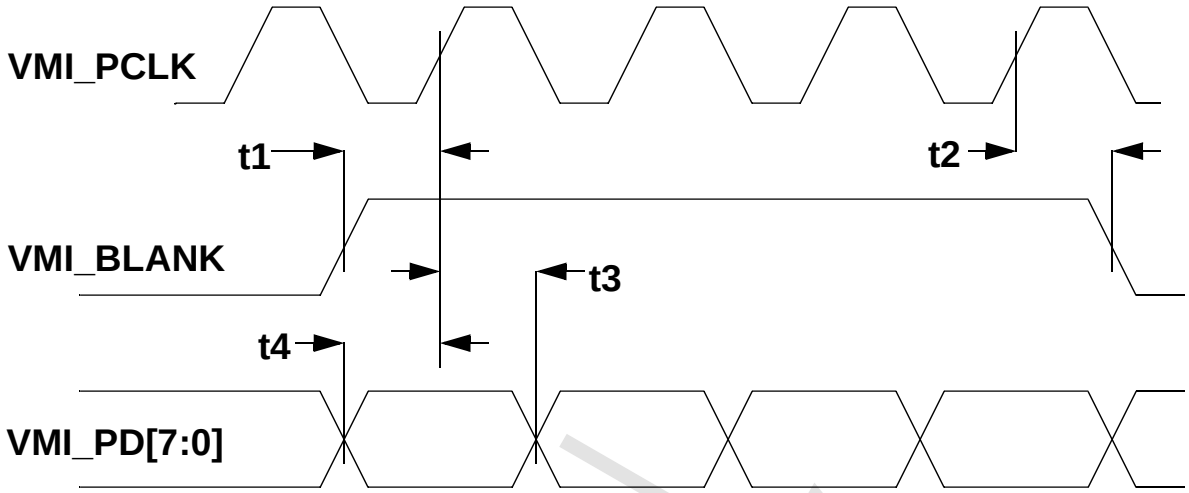


Figure 10.10 VMI Video In Waveforms

Table 10.16 VMI Video In Timing

Symbol	Parameter	Min	Max	Units
t1	VMI_BLANK (VACTIVE) setup to VMI_PCLK high	5	-	ns
t2	VMI_BLANK hold after VMI_PCLK high	0	-	ns
t3	VMI_PD[7:0] hold after VMI_PCLK high	0	-	ns
t4	VMI_PC[7:0] setup to MVI_PCLK high	5	-	ns

10.12 Digital RGB Out Timing

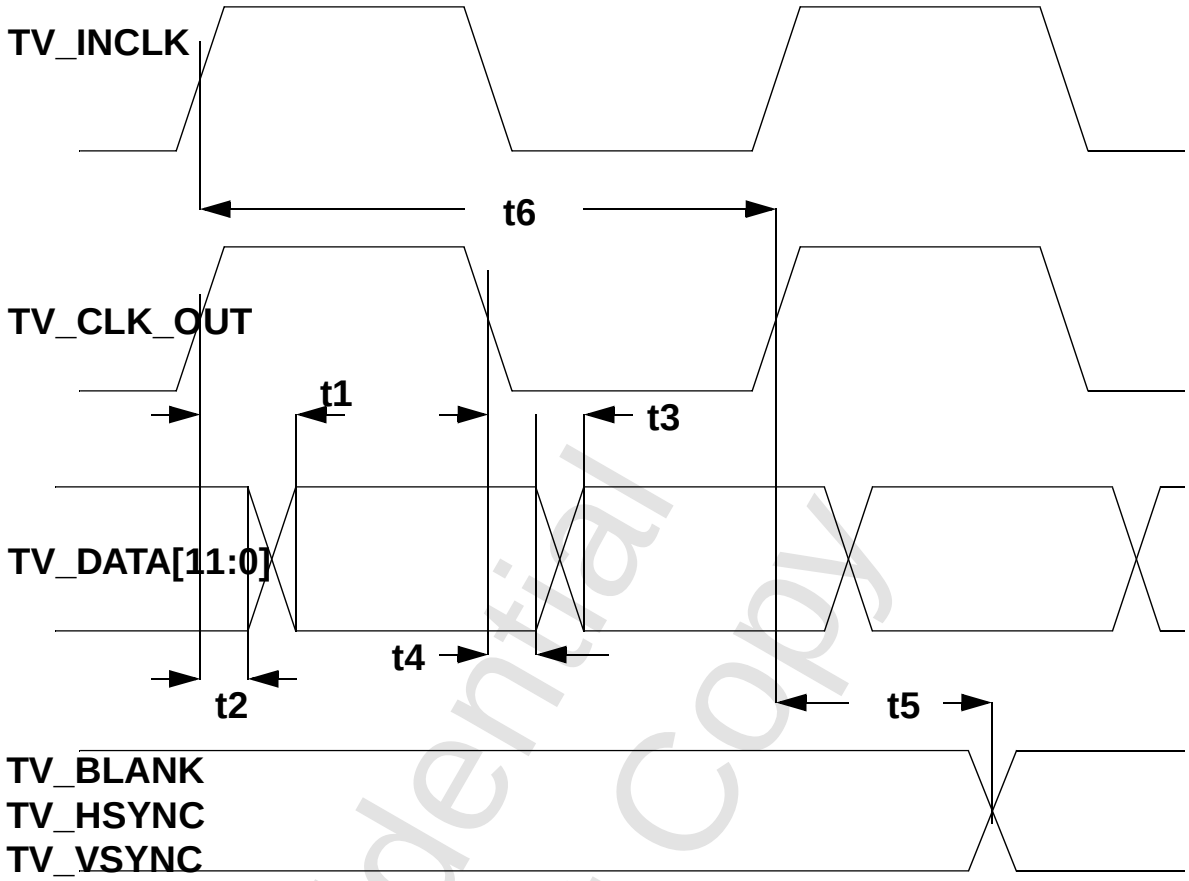


Figure 10.11 Digital RGB Out Waveforms

Table 10.17 Digital RGB Out Timing

Symbol	Parameter	Min	Max	Units
t1	Positive Clock Out to next Digital Data valid	-	tbd	ns
t2	Positive Clock Out to current Digital Data invalid	tbd	-	ns
t3	Negative Clock Out to next Digital Data valid	-	tbd	ns
t4	Negative Clock Out to current Digital Data invalid	tbd	-	ns
t5	Clock to Controls delay	-	tbd	ns
t6	Relationship between TV_INCLK and TV_CLK_OUT (Slave Mode only)	tbd	tbd	ns

10.13 ROM Read Cycle

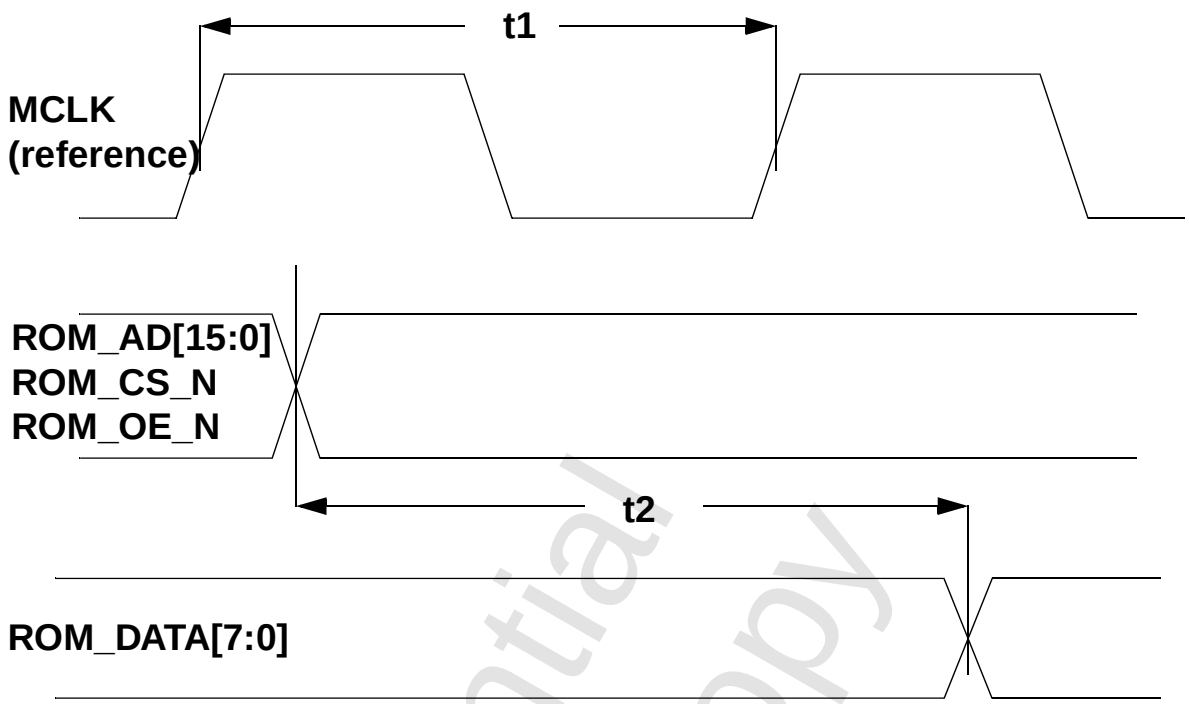


Figure 10.12 ROM Read Cycle Waveforms

Table 10.18 ROM Read Cycle

Symbol	Parameter	Min	Max	Units
t1	MCLK Period (Reference)	-	-	ns
t2	ROM_AD[15:0] to Data Valid	-	tbd	t1
t2	ROM_CS_N to Data Valid	-	tbd	t1
t2	ROM_OE_N to Data Valid	-	tbd	t1

10.14 ROM Write Cycle

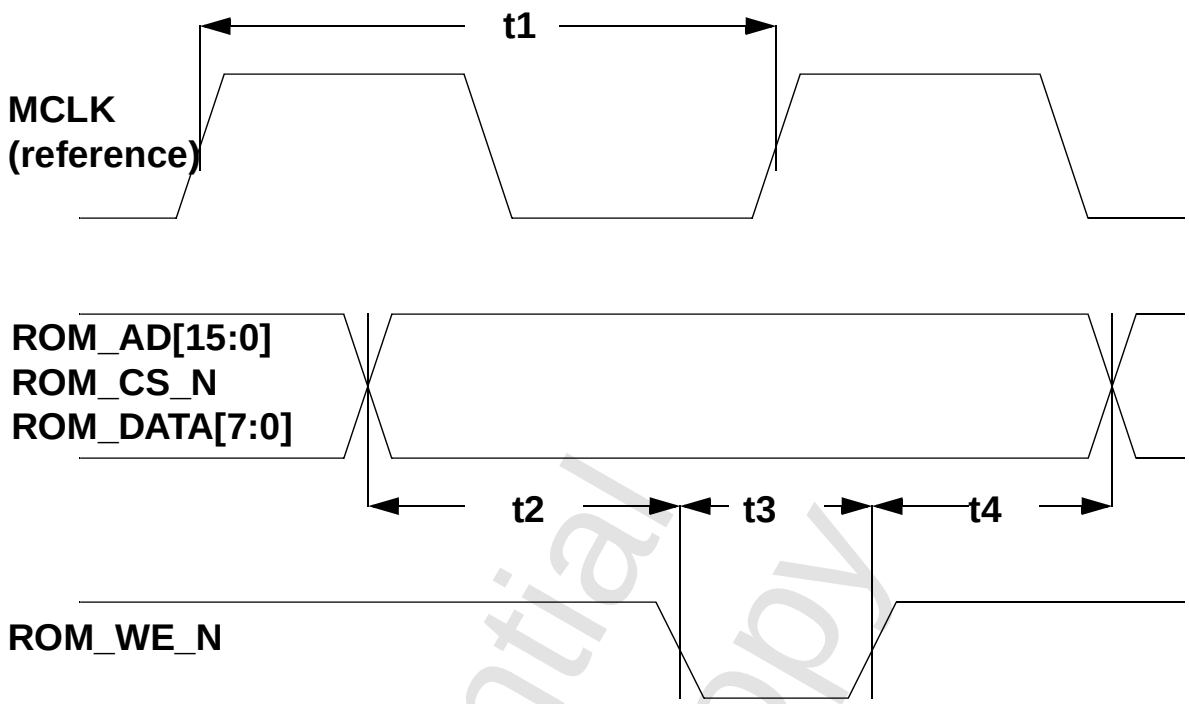


Figure 10.13 ROM Write Cycle Waveforms

Table 10.19 ROM Write Cycle

Symbol	Parameter	Min	Max	Units
t1	MCLK Period (Reference)	-	-	ns
t2	ROM_AD[15:0] to ROM_WE_N active	-	tbd	t1
t2	ROM_CS_N to ROM_WE_N active	-	tbd	t1
t2	ROM_DATA[7:0] to ROM_WE_N_active	-	tbd	t1
t3	ROM_WE_N Active low pulse width	-	tbd	t1
t4	ROM_AD[15:0] hold from ROM_WE_N inactive	-	tbd	t1
t4	ROM_CS_N hold from ROM_WE_N inactive	-	tbd	t1
t4	ROM_DATA[7:0] hold from ROM_WE_N inactive	-	tbd	t1

11 Package

11.1 Introduction

The Voodoo3 is supplied in a 352-pin 35-mm BGA package with 100 thermal balls (total of 452 balls).

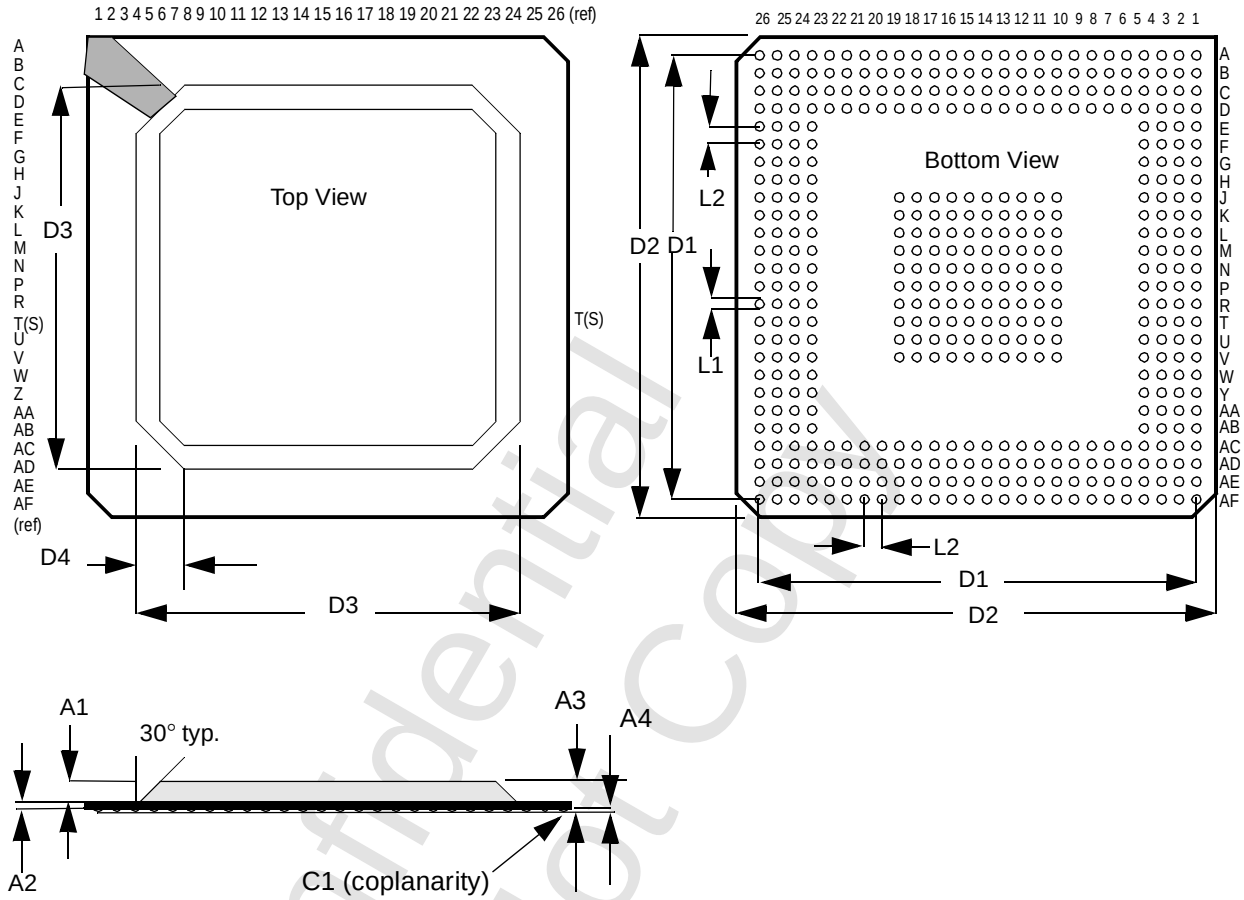


Figure 11.1 Physical Dimensions

Symbol	Minimum (mm)	Nominal (mm)	Maximum (mm)
A1		1.17 ref	
A2		0.56 ref	
A3	2.20	2.33	2.46
A4	0.50	0.60	0.70
C1		0.15	
D1		31.75	
D2	34.80	35.00	35.20
D3		30.00 ref	
D4		4.00	
L1	0.60	0.75	0.90
L2		1.27	

Pads on the PC board may be placed as shown in Figure 11.2.

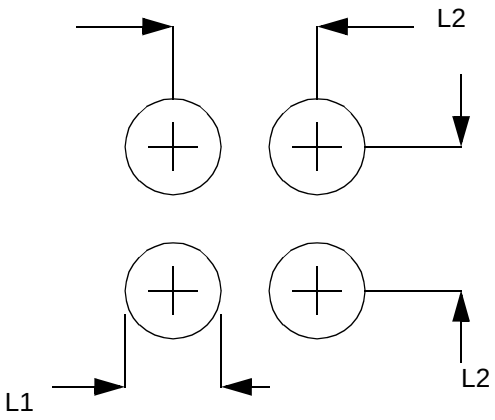


Figure 11.2 Pad Layout

Symbol	Minimum (mm)	Nominal (mm)	Maximum (mm)
L1		0.71	
L2		1.27	